High Voltage Engineering Techniques For Space Applications

Day 1 of 2

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April 2-3, 2012

Appreciation…

- *First and foremost, thanks to you all for making the effort to come. I sure hope we put on a fun and useful workshop for you!*
- *Special thanks to Dave Kusnierkiewicz and APL as our hosts for providing this fantastic facility. Thanks also to Sandy Rosenberger, Brad Carson, Bill Ligget, LaTosha Hill and John Sommerer of APL for their time and effort in making this event happen so smoothly.*
- *Personal thanks to Eric Young, Denney Keys and, in particular, Julian Ramirez of GSFC for their guidance and great support.*
- *And… thanks to our NESC friends, in particular Hope Venus and Ian Batchelder, for their support with the preparations for this meeting and their efforts to provide a quality webcast.*

2 + 2 = 4 Day Strategic Plan…

- *The complete seminar consists of two 2 day sessions with the first 2 days here at APL and the subsequent 2 days at JPL in October (tentatively on 10/22-23).*
- *The two sessions are stand-alone although complementary.*
  - ***This session concentrates on theory, component application and design practices.***
  - ***October session will consist of discussing 5-6 specific flight design cases covering a range of applications.***
  - ***A detailed and useful report from this session will come out in the June-July timeframe.***

2 Day Timeline

Start time	DAY 1 TOPIC
0830	INTRODUCTORY STUFF
0845	GROUNDWORK FOR DISCUSSIONS
0900	APPROACH TO HIGH RELIABLE HIGH VOLTAGE SYSTEM DESIGN- PART 1
0955	**BREAK**
1005	APPROACH TO HIGH RELIABLE HIGH VOLTAGE SYSTEM DESIGN- PART 2
1120	**QUESTIONS/DIALOGUE**
1200	**LUNCH**
1300	OVERVIEW OF HIGH VOLTAGE COMPONENTS AND TECHNOLGIES
1330	HIGH VOLTAGE CAPACITOR TUTORIAL
1350	HIGH VOLTAGE RESISTOR TUTORIAL
1405	HIGH VOLTAGE CONNECTORS AND CABLES
1440	**BREAK**
1450	**QUESTIONS/DIALOGUE**
1535	HIGH VOLTAGE INSULATORS AND ELECTRIC FIELD CONTROL TECHNIQUES
1635	E-FIELD ANALYSIS METHODS AND SOFTWARE
1700	**QUESTIONS/DIALOGUE**
1730	**RECEPTION**
1900	**ADJOURN**

Start time	DAY 2 TOPIC
0830	INTRODUCTORY STUFF
0840	LEIDECKER ON WIEBULL METHODS
0900	HENNING LEIDECKER'S GALLERY OF FAILURES
0915	SYSTEM DESIGN CHOICES- PART 1 - CLEANING AND CONTAMINATION - VENTING CONSIDERATIONS - CHOICE OF INSULATING MEDIA - PREFERRED ENGINEERING PLASTICS - OTHER SOLID INSULATING MATERIALS - ENCAPSULATION METHODS
1015	**BREAK**
1025	SYSTEM DESIGN CHOICES- PART 2 - SHIELDING APPROACHES - INSULATING COATINGS - GROUNDING APPROACHES - PC BOARD DESIGN CONSIDERATIONS - HIGH VOLTAGE SOLDER JOINTS - PACKAGING AND CONSTRUCTION
1135	ELEMENTAL DESIGN APPROACHES- PART 1 - OSCILLATOR DESIGN
1200	**LUNCH**
1240	ELEMENTAL DESIGN APPROACHES- PART 2 - MAGNETICS DESIGN AND MANUFACTURE - HIGH VOLTAGE MULTIPLIER DESIGN - MONITOR AND FEEDBACK APPROACHES - REGULATORS AND MODULATORS - OUTPUT FILTER DESIGN APPROACHES - OUTPUT TERMINATION APPROACHES - HIGH VOLTAGE CABLES - MATCHING UP TO THE "USER" END - "SHRINKING" A DESIGN
1515	**BREAK- EARLY ADJOURN POINT**
1530	**QUESTIONS/DIALOGUE**
1600	MEASUREMENT METHODS
1630	OTHER IMPORTANT STUFF - RADIATION EFFECTS - GSE AND SIMULATOR DESIGN - SAFETY IS ALWAYS FIRST - SUMMARY THOUGHTS - PLANNING FOR OCTOBER
1730	**QUESTIONS/DIALOGUE**
1800	**ADJOURN**

Thanks to Special Visitors…

- *We have several vendors who specialize in the high voltage business who have come to participate.*
  - ***CalRamic Capacitors***
  - ***Ohmcraft Resistors (Micropen)***
  - ***Teledyne-Reynolds***
  - ***Micropac***
  - ***RJR***
- *Many of you also know Eric Hertzberg and Dr. Henning Leidecker. Eric will be speaking later today and Henning will speak tomorrow morning.*

Dedications…

- *Scientists and Engineers in aerospace are the product of both what they learn and who has taught them. My own personal and professional thanks goes to:*
  - ***John Maurer (Michigan)***
  - ***Art Ruitberg (GSFC)***
  - ***Helmut Rosenbauer (Max Planck Institute)***
  - ***Eric Hertzberg (Lockheed)***
  - ***Tom Sanders (Lockheed)***
  - ***Doug Simpson (Lockheed)***
  - ***Henning Leidecker (GSFC)***
  - ***Bill Dunbar (Boeing)***

A Surprising Space Fact…

Fact: *All of the equipment launched in the 55 year history of the space program equates to less than 1 day of worldwide auto production.*

Conclusion: *At a fundamental level, statistical process control principles associated with mass production do not apply to the space business.*

Lesson: *The space workforce is fundamentally a craft-based "guild" where key knowledge is passed from generation to generation.*

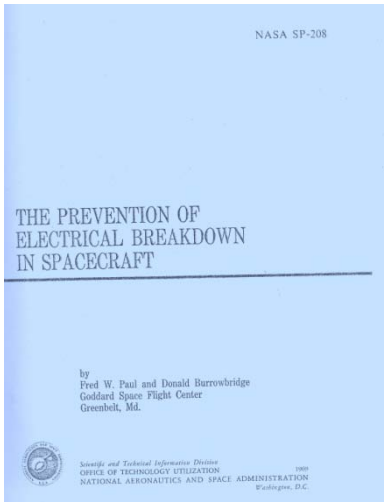
Our Starting Point…

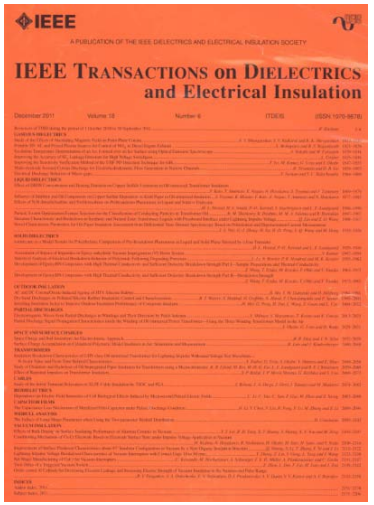
- *4 years ago I committed myself to giving back 20% of my work time to the country by doing teaching and mentoring on engineering.*
- *It is my way of "**paying back by paying forward"** for the benefit of the next generation of engineers in our profession.*
- *When Eric Young approached me a year ago about doing this high voltage engineering workshop I thought it would be a fun and useful way of making good on a part of my commitment.*
- *So here we are… There are many rules and rule books plus other excellent informational resources related to the development of high voltage systems. However, very few provide a practical **connection between the "how to" and the "here's why"**.*
- *My personal hope during this workshop is to relate 35 years of mistakes and practical lessons learned in developing more than 50 different flight high voltage system designs.*

Becoming a High Voltage "Expert"…

- *The space hardware development business is best described as a learning process consisting of uncountable hours of slogging occasionally interrupted by a few exciting minutes of true insight.*
- *The **"pay back"** component of our time together is to share these key insights so that you will come away with a more complete understanding of what it takes to engineer reliable high voltage systems.*
- *The **"pay forward"** component is the hope that this effort can snag a few of young energetic engineers who are willing to commit themselves to the process of becoming the next generation of experts.*

High Voltage Resources…





But Wait… There's More!

- *Electronic Packaging and Interconnection Handbook, Charles A. Harper, McGraw-Hill, 2000*
- *J.C. Martin on Pulsed Power, J.C. Martin, Plenum Press, 1996*
- *High Voltage and Electrical Insulation Engineering, Ravindra Arora & Wolfgang Mosch, John Wiley and Sons, 2011*
- *Magnetic Components: Designs and Applications, Steve Smith, Van Nostrand Reinhold Company, 1985*
- *Handbook of Transformer Design and Applications, William M. Flanagan, McGraw-Hill, 1993*
- *Electroceramics, A. J. Moulson & J. M. Herbert, Chapman and Hall, 1993*
- *Passive Electronic Component Handbook, Charles A. Harper, McGraw-Hill, 1997*
- *High Voltage Engineering Fundamentals, E. Kuffel & W.S. Zaengal & J. Kuffel, Newnes, 2001*
- *High Voltage Vacuum Insulation: Basic Concepts and Technological Practice, Rod Latham, Academic Press, 1995*
- *Partial Discharge Detection in High-Voltage Equipment, F.H. Kreuger, Anchor Press, 1989*

… and More!

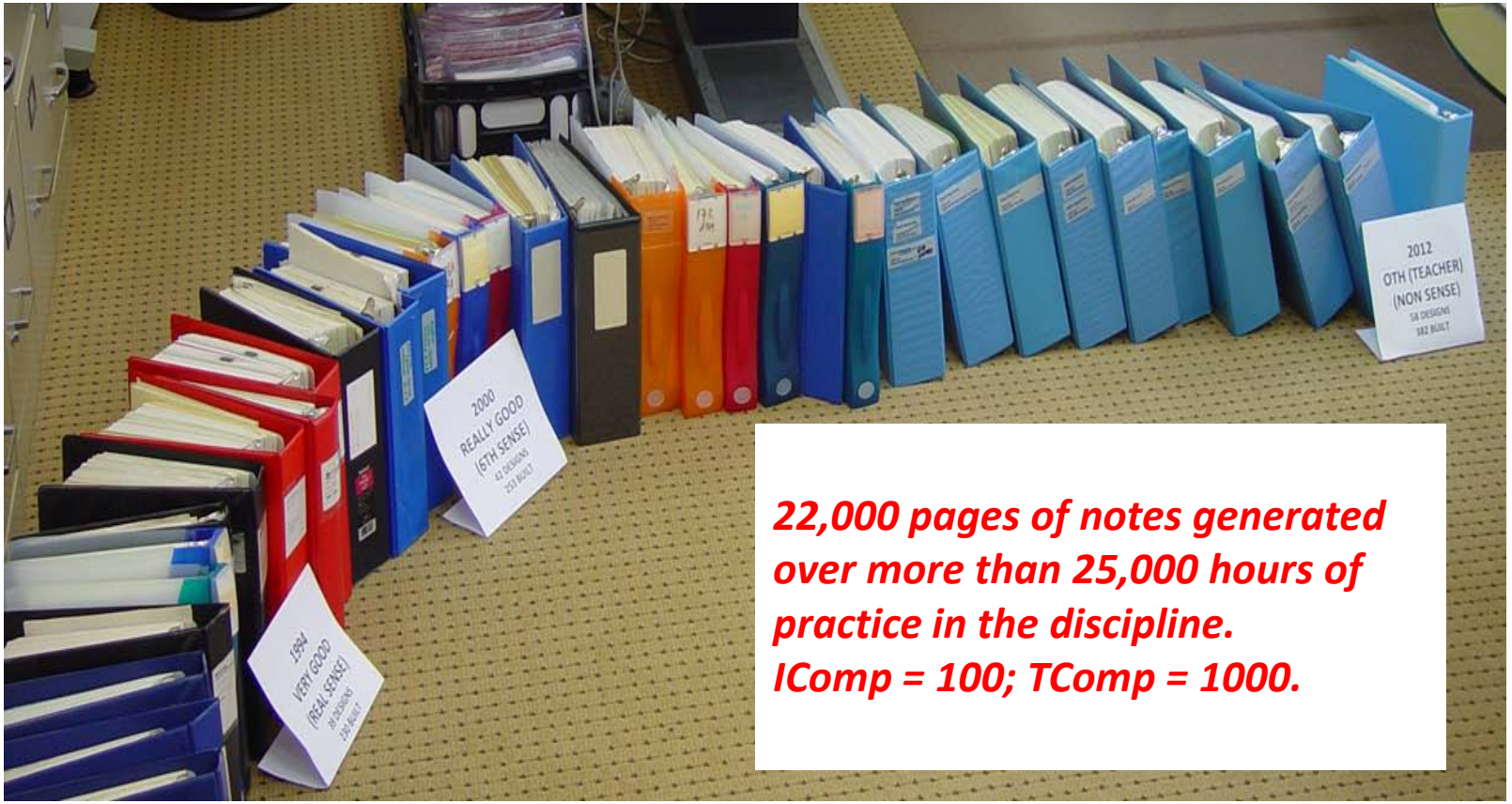
- *Handbook of Electrical and Electronic Insulating Materials, W. Tillar Shugg, IEEE Press, 1995*
- *Microwave Tubes, A. S. Gilmour, Jr., Artech House, 1986*
- *Dielectric Phenomena in High Voltage Engineering, F. W. Peek, Jr., Rough Draft Printing, 1915 (2008)*
- *Corona Onset Voltage of Insulated and Bare Electrodes in Rarified Air and Other Gases, W. G. Dunbar, 1966*
- *Design Guide: Designing and Building High Voltage Power Supplies, W. G. Dunbar, 1988, Volumes I-II*
- *Space Transportation System Orbiter Upgrades Program: Electrical Auxilary Power Unit (EAPU) Corona Design Guideline, 2000*
- *High Voltage Design Criteria, MSFC-STD-531, 1978*

There are also JPL and NASA Design Rules and documents and handbooks that I have not cited but are also useful and consistent with what is presented.

You Learn From Your Mistakes…
The Early Years *(7000 pages)*

You Are What You Learn…
The Middle Years (8000 pages)

You Become What You Remember… End of the Line and OTH (7000 pages)



22,000 pages of notes generated over more than 25,000 hours of practice in the discipline.
IComp = 100; TComp = 1000.

Core Message…

- *Reality is more complex than theory**! It takes time, patience and perseverance** (and good notes) to become an expert at translating the right set of key physics and engineering principles into high voltage "art".*
- *Practitioners must have a broad understanding of physics, engineering principles, materials and component technologies if reliable optimal designs are to be achieved.*
- *A long-term institutional commitment is required if an expert engineering team is to be developed and then sustained.*
- *An engineering team should develop 1-2 designs per year over if its expertise is expected to grow and remain current.*

Achieving "Goodness" in a Design…

- ***Become a master the "elements"*** *we will be discussing.*
- ***Constantly learn and improve by constantly doing.***
- ***Value mentoring as a two-way mode of engineering interaction*** *with the goal of achieving creative ideas, simplified designs and optimized implementations.*
- *At a personal level, develop the* ***ability to critically self-assess as part of the design process*** *(inside-out pressure).*
- *At an institutional level develop* ***the ability to be self-critical as part of the review process*** *(outside-in pressure).*

The Approach…

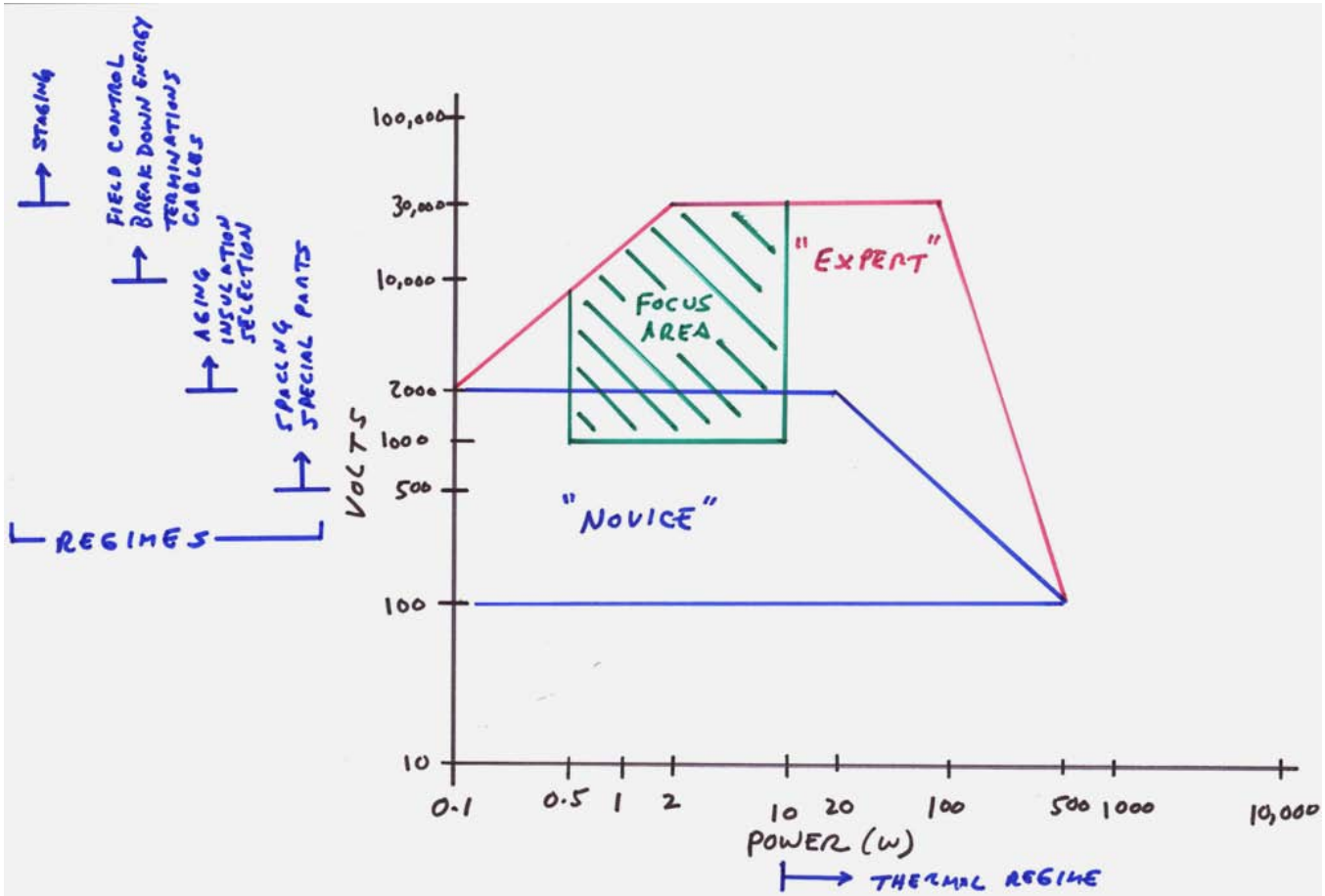
The views expressed here are entirely my own and do not reflect the views of NASA management or any rational person!

- *The design and implementation approaches presented here are based on a personal perspective and personal approach developed over 35 years of practice in the field.*
- *There are many other equally good approaches so look at this recipe as one means of achieving a "connected" and reliable design.*
- *The key to any successful approach is to ensure that it is derived from correct physical principles that have been systematically investigated and understood.*
- *Hopefully by presenting the details of my approach you can then apply some of the ideas to your own designs.*

Types of High Voltage Systems…

- *Although the design considerations are similar or even identical over a wide range of high voltage system applications, we will be concentrating on smaller high voltage systems in the 0.5 to 10 watt range used in single output and multiple output instrumentation applications.*
  - ***Detector Bias Systems (Silicon, CEM, MCP etc.)***
  - ***Mass Spectroscopy/Time of Flight***
  - ***Spacecraft Charge Control***
  - ***Propulsion and Special Instrumentation Applications***

The High Voltage "Scale"…



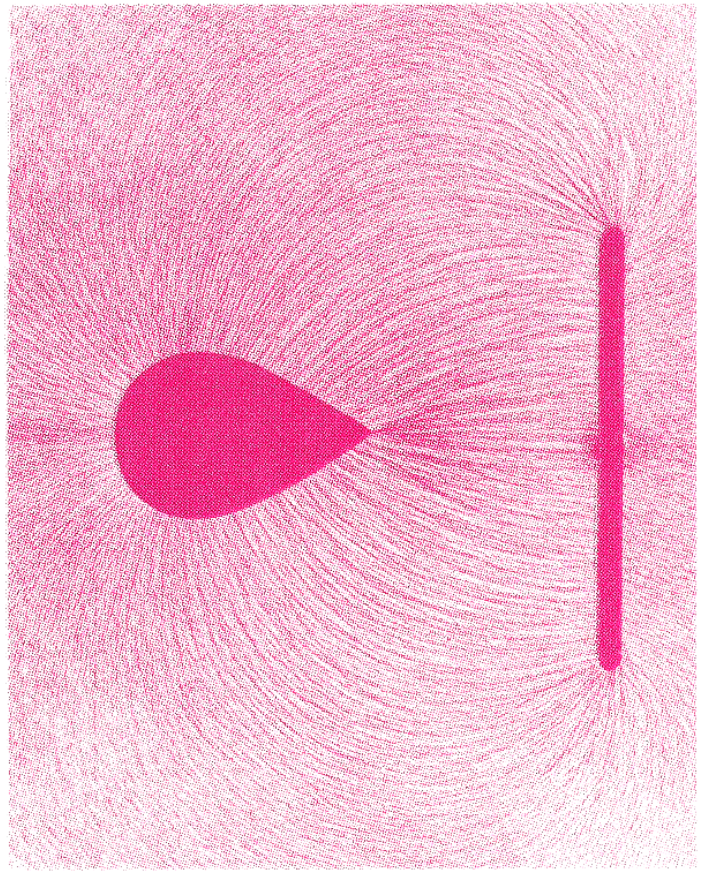
The Equation…

Maxwell's Electric Field Equation is Gauss's Law for the Electric Field described in differential form.

$$\nabla \cdot \mathbf{E} = \frac{\rho}{\varepsilon_0}$$

In the electrostatic case the Electric Field can be expressed in a more useful form as the gradient of the electrostatic potential.

$$E = -\nabla V$$



The Physics of High Voltage Breakdown…

- *Eric Hertzberg will talk more on the details later but it is important to geometrically manage the relationship between V, E, and relative permittivity with an insulating medium.*
- *The simple view is that the reliable generation of high voltage is dependent on limiting the resulting E-Field stress as expressed by the localized voltage gradient created in the isolating dielectric medium.*
- *Failure to properly manage the E-Field stress via geometry, spacing, material selection and control of defects can result in immediate voltage breakdown or time dependent dielectric failures depending on many primary and secondary factors.*
- *High voltage systems for space often have an additional dielectric issue associated with the need for both ground operations vs. space operations that must also be managed to assure that ground operations do not reduce in-space reliability.*

Some Definitions… 1

- **Arc-** A self-sustaining electrical discharge.
- **Breakdown-** The temporary or permanent loss of normal insulating properties by a dielectric material.
- **Corona-** Luminous usually localized discharge with a low current flow due to a deionization release of energy. Typically a "point" breakdown with a negative electrode and a "film" breakdown with a positive electrode.
- **Discharge-** Any conducting mechanism between two electrodes separated by a dielectric.
- **Flashover-** A discharge around or over the surface of a liquid or solid dielectric.
- **Field Emission-** Current emitted from an electrode (typically a point).

Some Definitions… 2

- **Multipactor-** Breakdown in hard vacuum at certain RF frequencies and in certain geometries due to secondary emission of electrons.
- **Partial Discharge-** Localized discharge due to transient gaseous ionization within an insulating system typically due to gaps or voids in combination with a dielectric transition.
- **Surface Breakdown-** Development of conducting channels between two electrodes on a conducting surface.
- **Surface Leakage-** Passage of current over the boundary surface of an insulator.
- **Tracking-** Development of conducting channels primarily on a dielectric surface where the surface is damaged by the process.
- **Treeing-** A cumulative failure where hollow channels branch slowing through a dielectric material resulting in permanent failure.

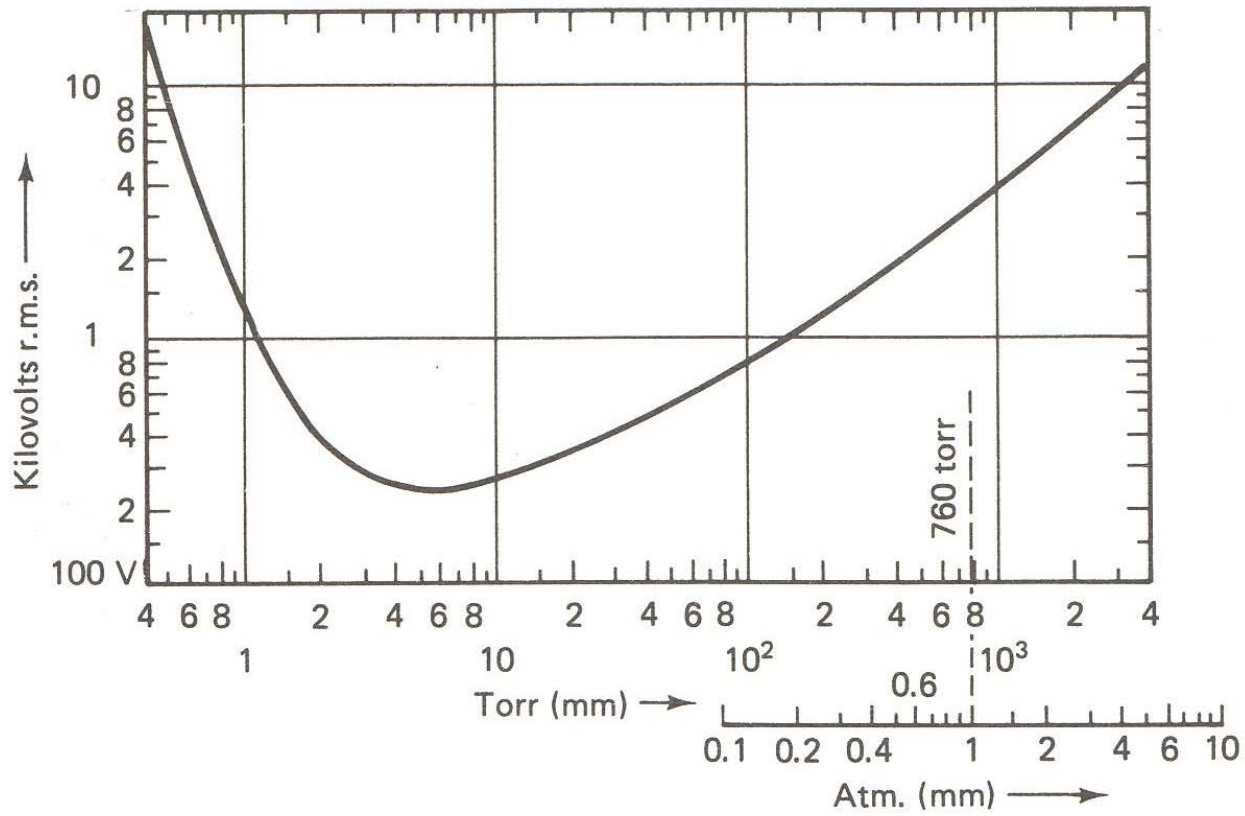
Intrinsic Dielectric Strength Limits…

- *The breakdown of Gasses at **STP** is dependent on type.*
  - *Air : ~3 kV/mm (75 V/mil)*
  - *He : ~0.37 kV/mm (9.3 V/mil)*
  - *SF_6 : ~9 kV/mm (222 V/mil)*
- *High Vacuum breakdown is surface and configuration dependent but is in the range of 20 to 40 kV/mm (500 to 1000 V/mil)*
- *Ignoring surface effects, Liquids and Solids bulk properties are generally similar in the same range of 15 to 20 kV/mm (375 V/mil to 500 V/mil).*

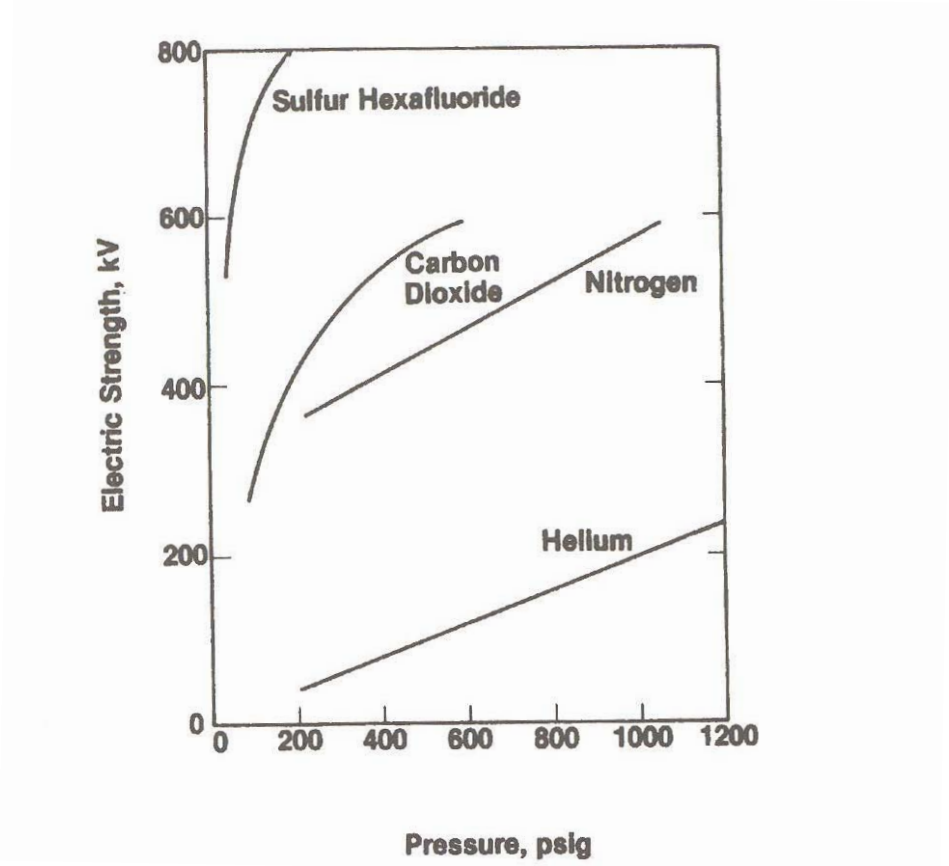
Operational Dielectric Strength Limits…

- ***Maximum** recommended DC design voltages:*
  - *Vacuum gaps: 3 kV/mm in general; lower preferred*
  - *Along insulator surfaces: 1 kV/mm*
  - *Within bulk insulator material: 4 kV/mm **(depends on life requirement; thermal runaway also ignored)***
  - *In atmosphere at **STP**: 1.5 to 2 kV/mm*
- *Stay tuned…There is much more to this story!*

Paschen Curve for Air…

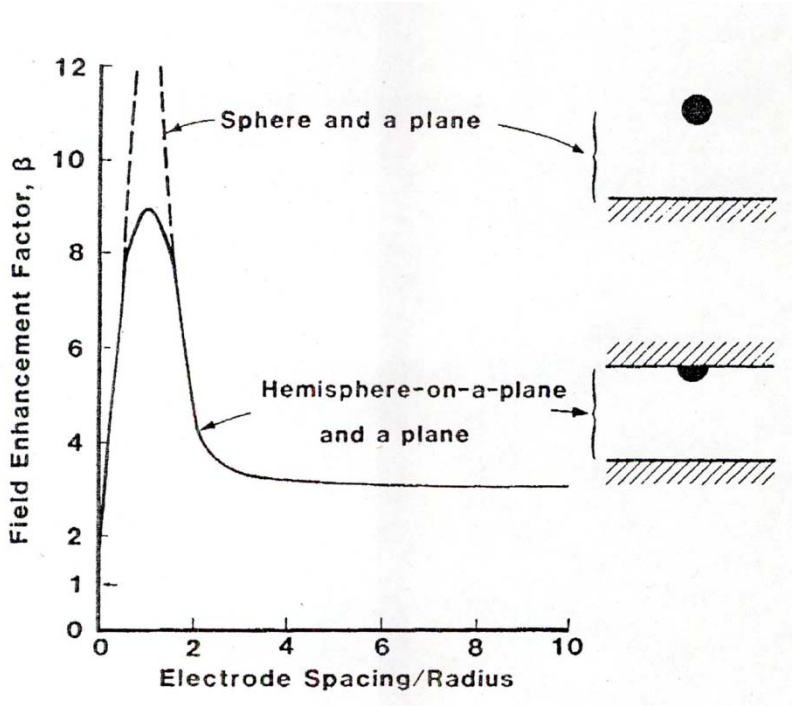


Affect of Pressure…

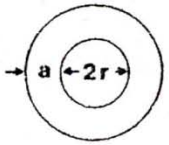
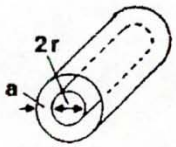
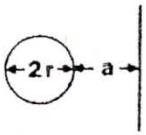
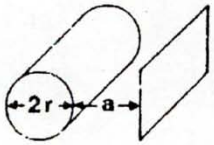
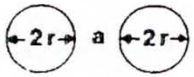
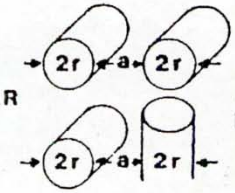


Geometry and the E-Field…

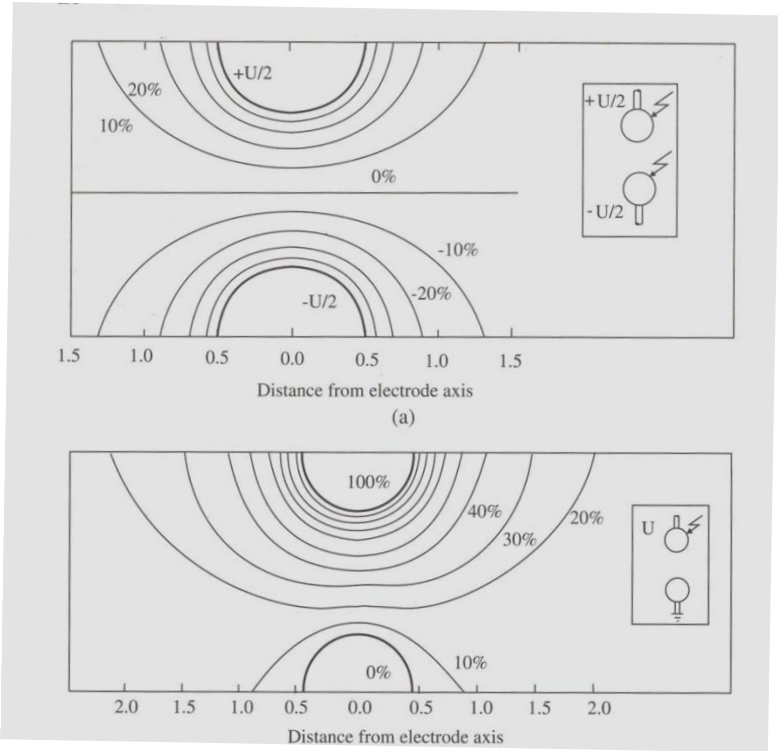
- *Simple factors do not tell the entire story of dielectric breakdown since geometry of the conductors play a strong role.*
- *In carefully designed systems B_{eta} is generally 3 or lower.*

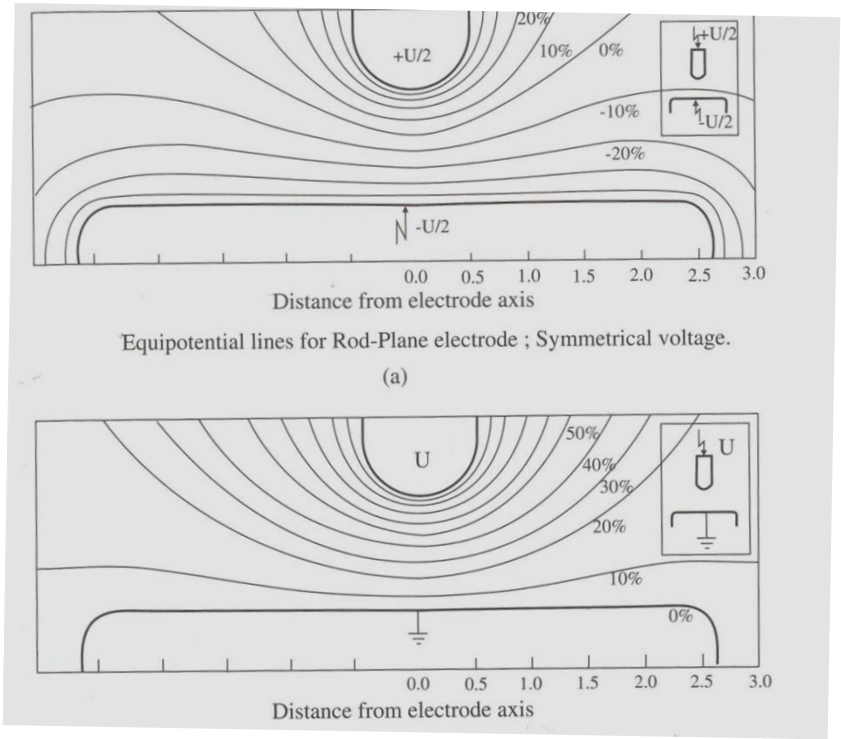


Simple Examples of E-Field Enhancement…

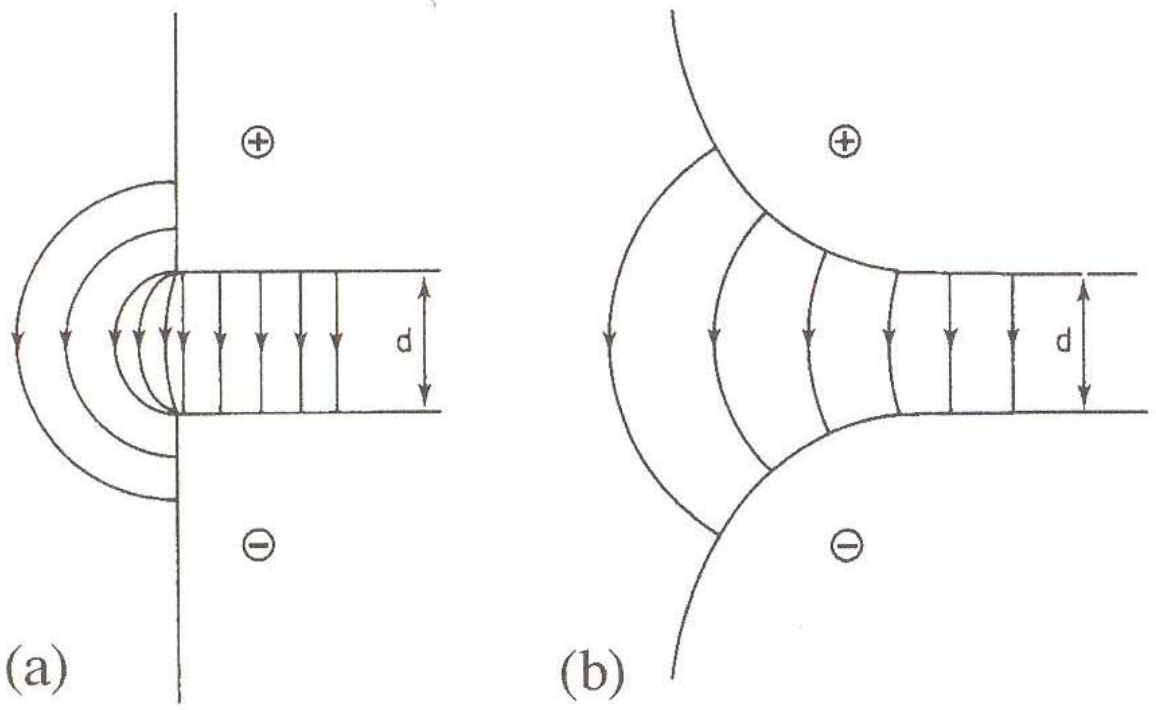
Configuration		β	Configuration		β
CONCENTRIC SPHERES		$1 + \frac{a}{r}$	COAXIAL CYLINDERS		$\frac{\frac{a}{r}}{\ln(1 + \frac{a}{r})}$
SPHERE AND PLANE		$0.9(1 + \frac{a}{r})$	CYLINDER AND PLANE		$\frac{0.9\frac{a}{r}}{\ln(1 + \frac{a}{r})}$
TWO SPHERES		$0.9(1 + \frac{a}{2r})$	PARALLEL OR PERPENDICULAR CYLINDERS		$\frac{0.9\frac{a}{2r}}{\ln(1 + \frac{a}{2r})}$

Effect of Asymmetrical Potential…





Effect of Poor Field Control…



AC and DC Gradients Act Different…

- *AC (top) and DC (bottom) gradient stress manifest themselves through capacitive and resistive ratios.*
- *DC gradients also have a time constant that must be managed especially in bi-polarity cases where space charge can amplify the field intensity.*
- *Matching up materials in an insulating stackup is important for both mechanical and electrical reasons.*

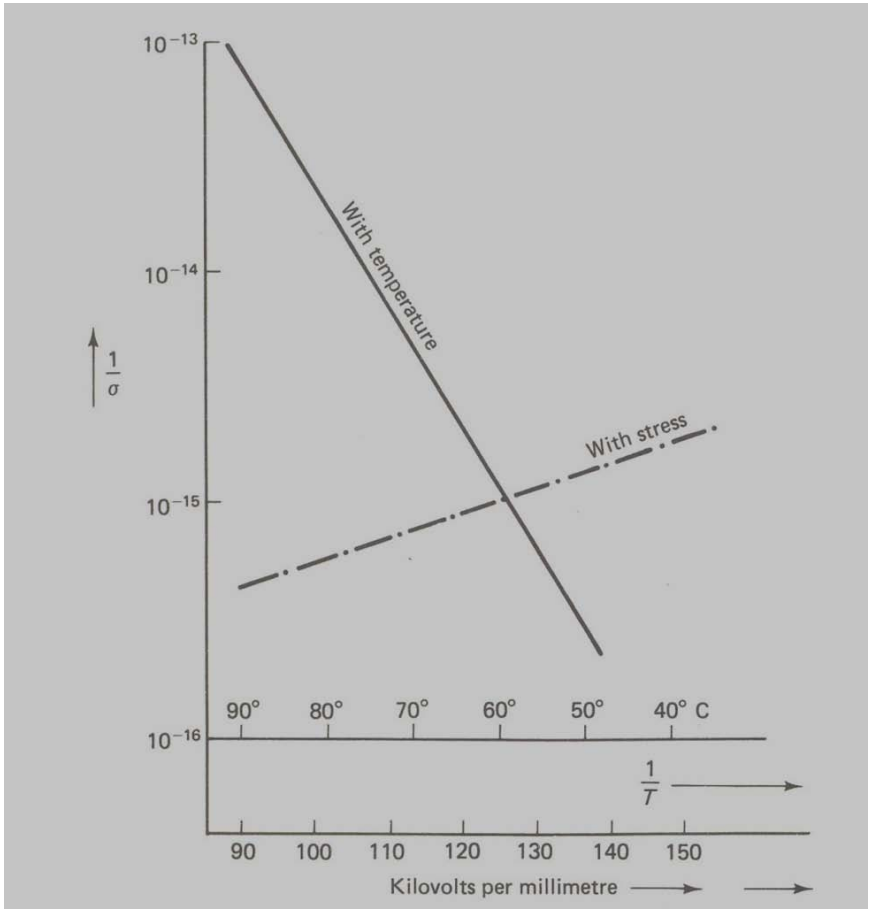
$$G_x = \frac{E}{\varepsilon_x(T_1/\varepsilon_1 + T_2/\varepsilon_2 + \ldots + T_n/\varepsilon_n)}$$

where
E = Total voltage across all insulation
G_x = Gradient (electric stress) in V/mil
T = Thickness in mils
ε = Dielectric constant

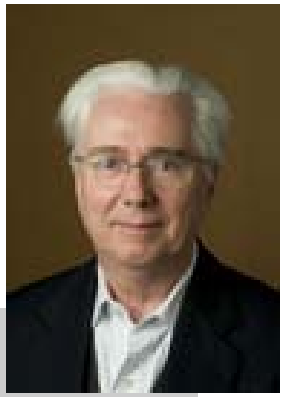
$$G_x = \frac{\rho_x E}{(T_1\rho_1 + T_2\rho_2 + \ldots + T_n\rho_n)}$$

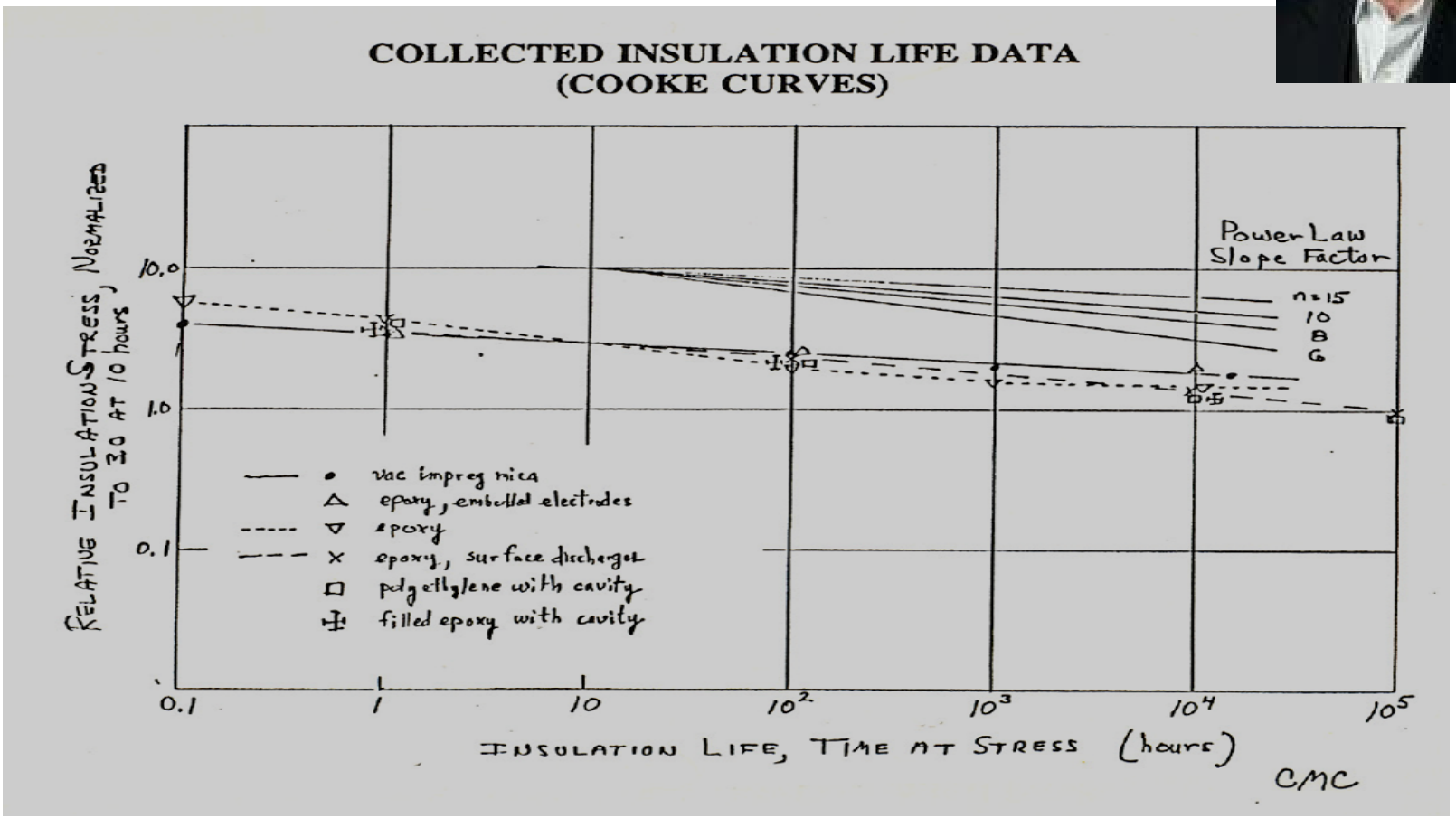
where
E = Total voltage across all insulation
G_x = Gradient (electric stress) in V/mil
T = Insulation thickness in mils
ρ = Volume resistivity
Subscript $x = 1, 2, \ldots, n$

Effect of Temperature and Voltage on Insulator Volume Resistivity…

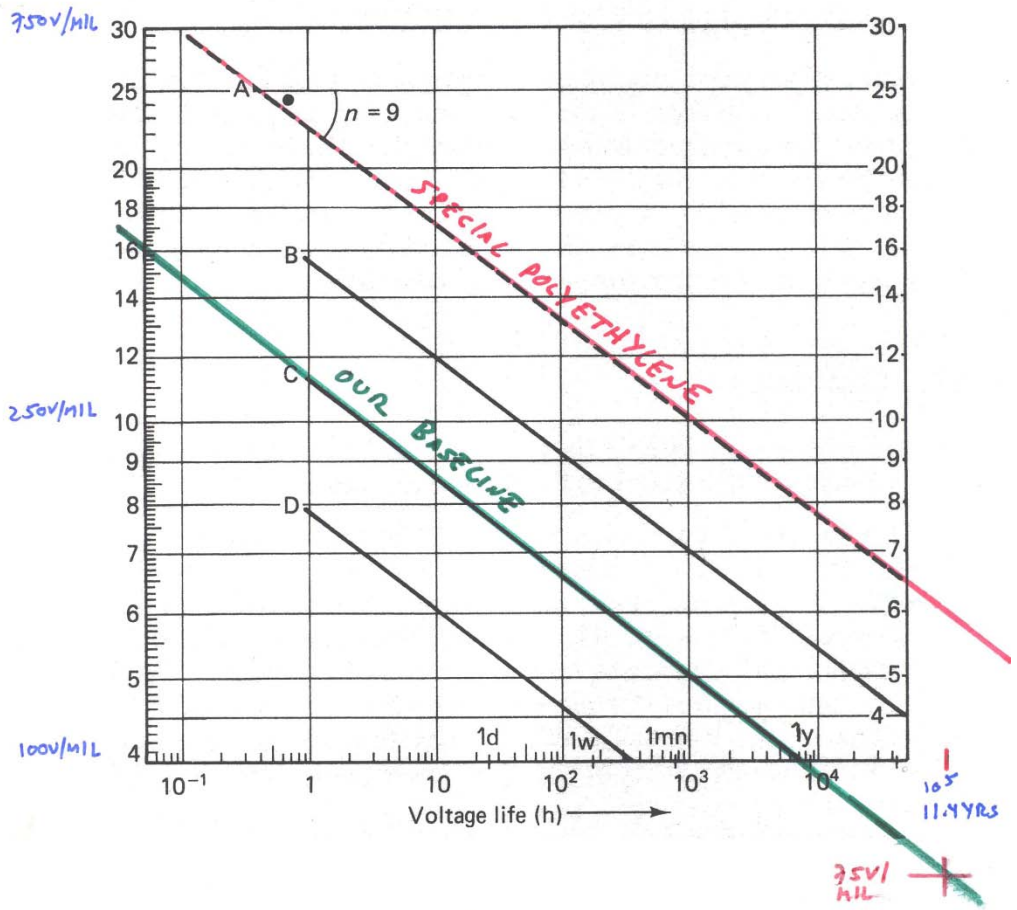


The "Eureka" Moment *(1986)*...





9th Power Aging Curve…



Managing the Race to Failure… 1

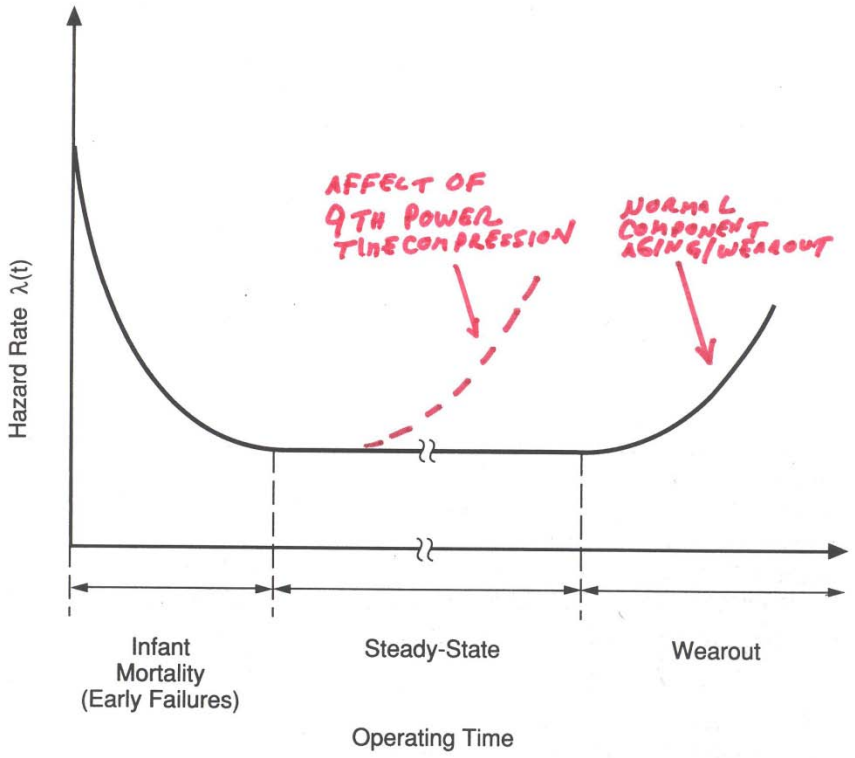
- *Many factors affect the performance and reliability of insulating media used in high voltage systems with the most important being E-Field stress, temperature, porosity and contaminants.*
- *Ceramics and Polymers are chemically different as well as different in their response to an electric field when used as a bulk dielectric.*
- *Plastic and epoxy polymer formulations are the most common building blocks for high voltage insulation systems.*
- *Required operating lifetime must be accounted for when derating dielectric materials.*

Managing the Race to Failure… 2

- *The "Infinite life" stress factors for polymers are in the range of **20 to 75 V/mil** with **50 V/mil generally considered to be a reasonable design value for a 10 year life.***
  - *Represents range of 10:1 and 7:1 ratio against dielectric strength limits.*
- *Voltage acceleration Factors vary but are generally considered to range between the 8^{th} and 10^{th} power with a **9^{th} power acceleration** considered a good value for most plastic dielectrics.*
- ***Defects can result in premature aging and/or failure** due to corona and/or partial discharges and must be accounted for in the design and processing.*
- *A dimensionally minimized design must account for the geometric amplification of E-Field stress as component spacing is reduced as well as the amplification effect of potential defects introduced by either design or process.*

Rethinking the "Bathtub Curve"…

- *Standard NASA reliability assumptions are predicated on the elimination of infant mortality through parts screening combined with process control and burn-in at the unit level.*
- *Unit wearout is considered to be far in the future resulting in a long steady-state lifetime.*
- ***E-Field stress-induced aging can result in a significant shortening of the steady-state life unless carefully managed in every susceptible element of a design.***

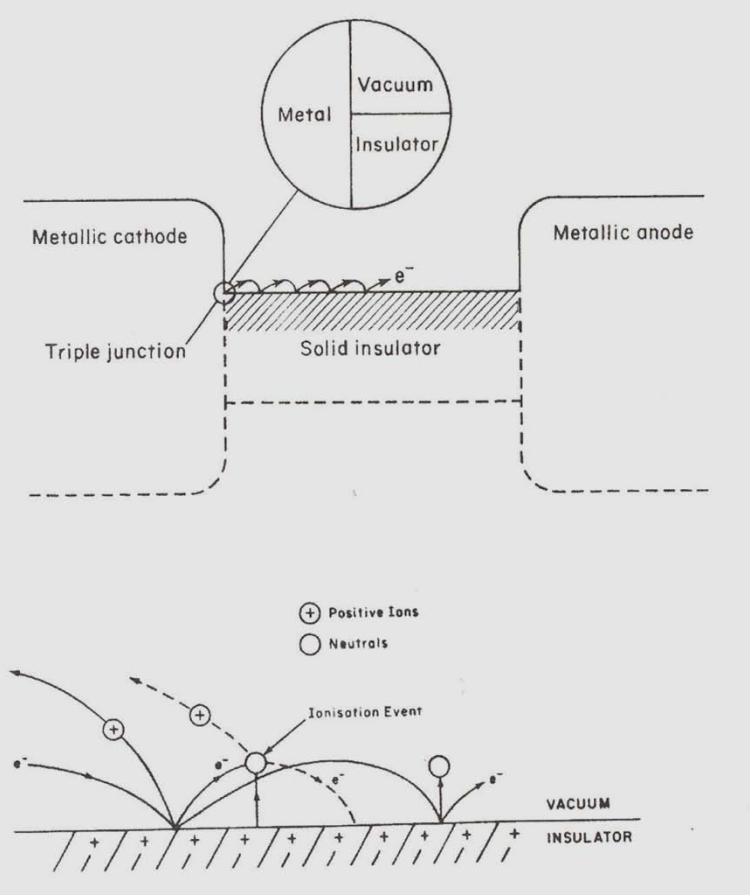


Formulating an Insulation Strategy…

- *System reliability will ultimately be set by the insulation strategy chosen for each system element in combination with the **true E-field stress ratio** and the quality of the processes used in implementation.*
- *Insulation strategy **must be achievable** as well as matched to operating and test regimes, lifetime requirement, field control approach, volume and mass constraints, thermal requirements, material restrictions and the **skill of implementer**.*
- *Insulation strategy may (and probably should) vary by system element with the intent of optimizing reliability of each element within its unique requirements and process constraints.*

Managing Flashover, Arcing and Corona…

- *Designs that appear derated often have a triple-junction creating a high field point as a source of electrons to initiate a cascade that results in flashover, arcing or corona.*
- *Eric Hertzberg will address design approaches for minimizing these effects within an insulation system.*

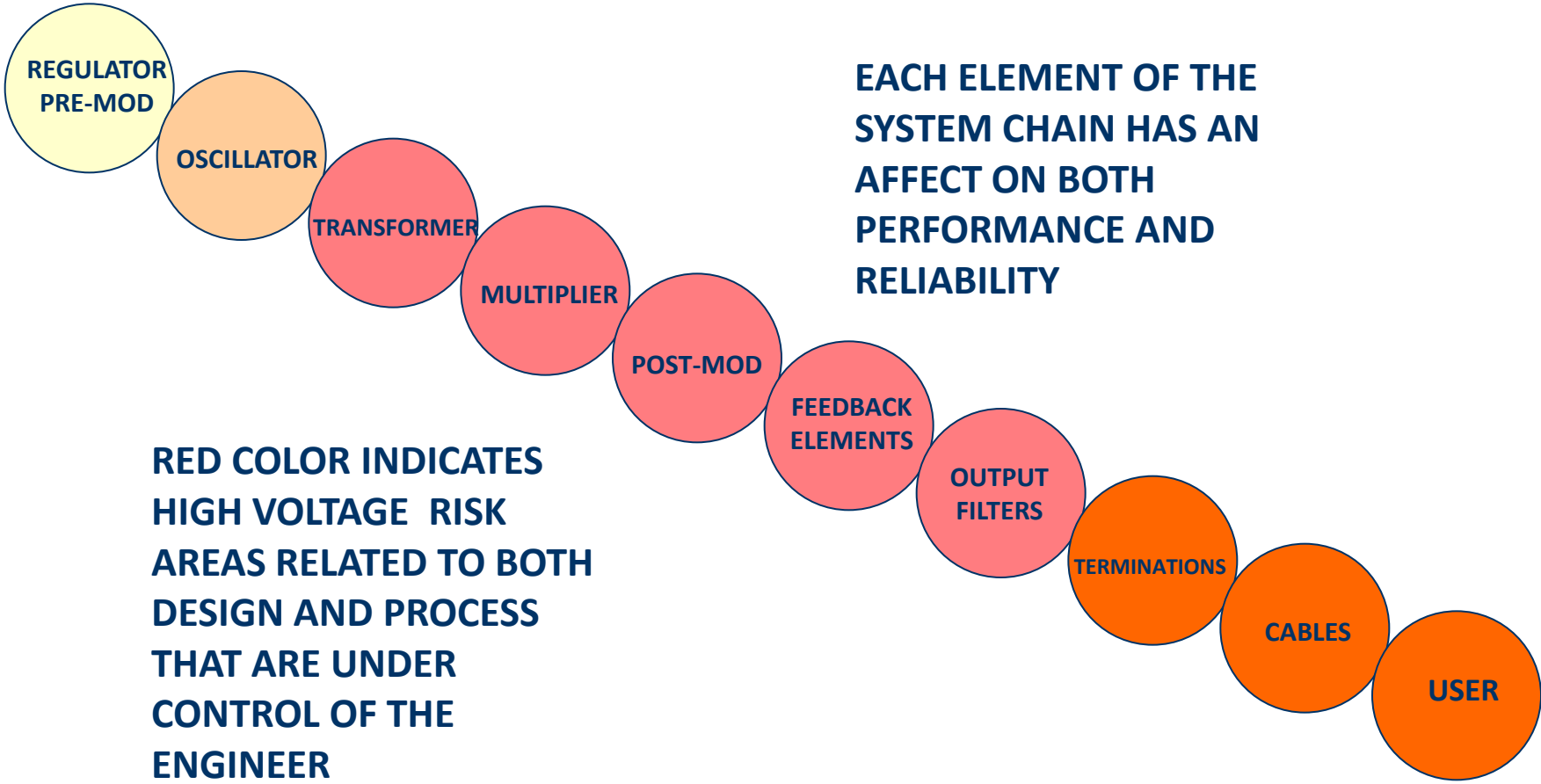


Progressive Design and Test Margins…

- *Testing can simply be pushing your design closer to failure such that survival does not necessarily mean the design is either qualified or reliable.*
- *Progressive design and test factors are essential to achieving a reliable and optimized design.*
  - *2X Margin for design*
  - **1.5X Margin for Accelerated Qual* ***($1.5^9 = 38$; 1 Yr = 10 days)***
  - *1.25X Flight Unit Over-Test and Operational Margin*
  - *1.0X Max Flight Operation*
- *1.25X flight operational margin can be traded for performance against life in some life extension scenarios.*

****Acceleration factors above ~1.5 may not yield trusted results due to secondary factors.***

The "Elemental" Picture…



EACH ELEMENT OF THE SYSTEM CHAIN HAS AN AFFECT ON BOTH PERFORMANCE AND RELIABILITY

RED COLOR INDICATES HIGH VOLTAGE RISK AREAS RELATED TO BOTH DESIGN AND PROCESS THAT ARE UNDER CONTROL OF THE ENGINEER

Achieving a "Connected" Design…

- *An **end-to-end "holistic" approach is essential** to the successful design, development, test and deployment of a reliable high voltage system.*
- ***Key requirements should be dissected and fully understood** within the performance and reliability trade space for the particular system.*
- *Each "element" of the design chain should be matched to the specific application and derived from **proven components and processes.***
- ***Push back on requirements to achieve simplicity** through the elimination of all non-essential elements.*

Connecting the Elements…

- *A reliable high voltage system design is the product of a systematic design approach where each system element is operated within its proven performance and reliability limits.*
- *Mixing and matching the system elements must be based on fundamental confidence derived from a combination of testing and experience.*
- *Extrapolations should be fully based on testing confirmed by appropriate analyses.*

Developing Confidence and Trust in Your Fundamental Processes…

- *"Heritage" is about applying trusted engineering techniques and process methods within an understood and appropriate operating regime.*
- *The fundamental elements and processes we will be discussing become your toolbox.*
- *Continuity in personnel, processes, components and test methods are the necessary basis of confidence and trust.*
- *End-to-end ownership of the design and participation in all key processes is essential for successful implementation.*
- *Total involvement also yields the comprehensive knowledge required to achieve future improvements.*

Why are we having problems? 1

- *Project and engineering organizations tend to encourage their experts to focus within a narrow discipline area rather than develop experience cutting across many disciplines.*
- *Organizational funding and training strategies are typically not consistent with the long-term commitment necessary to develop and maintain expert practitioners and the needed support facilities.*
- *Simulation-based design approaches together with reliance on marginally applicable risk-based (rather than physics-based) rule sets have resulted in engineers **at both the design level and review level** having relatively little practical experience dealing with the unique design and developmental challenges that occur in high voltage systems.*

Why are we having problems? 2

- *DOORS, as a system engineering tool, works best as a **"one-way"** top-down pathway for the development of requirements. Unless carefully done, it will not fully capture the unique cross-cutting design and reliability challenges that occur in high voltage designs. High voltage designs should be implemented in a **"two-way"** or **"up-down"** approach that achieves robustness through push-back and simplification.*
- *The above 4 drivers, combine to create requirements and associated designs that tend to over-reach the skill level of the designer. The potential consequence is the introduction of time-dependent failure modes that surface late in the development process, in the test process, or on-orbit.*

The TRL Dilemma…

- *TRL 6 readiness means nothing in a low production environment for high voltage systems except that the unit design at the beginning of its life built using standard processes can successfully survive the relevant flight environments.*
- *The heritage and development readiness of a high voltage system is rooted in the design, engineering and process robustness of the individual elements rather than in the high voltage system itself.*
- *High voltage systems are most reliable and also use the least system resources when they are uniquely engineered to be as simple and robust as practical for the specific application.*
- *Designs resulting in excess capability or that are excessively complicated are often less reliable (especially at the system level) and can use up system resources better spent in other areas.*

Seeking the Optimum Middle…

- *Requirements if worked in concert with a selected design approach can be enforced in ways that make the design implementation simpler or more complex (or both!).*
- *The designer must always seek the "optimum middle" by focusing on meeting key requirements while pushing back on everything else.*
- *Choose trusted design approaches and implementation methods and employ appropriate design and test factors.*
- *Design synthesis should match each element of the design to the requirements such that resources are applied in a way that balances system reliability between the elements.*
- *Focus on robust simple designs for all key hardware elements and across all key processes (parts, manufacture, testing, ops).*

Frequent Challenges…

- *Slow leaks in hollow resistors or other components.*
- *Use of film resistors in arc sensitive applications.*
- *Voids due to design or bonding delamination issues.*
- *Unvented volumes.*
- *Improper venting.*
- *Floating conductors and particles.*
- *Reliance on insulating properties of solder mask.*
- *Inadequate trace spacing.*
- *Unaccounted for field compression due to thermal gradients or space charge.*
- *PC board voids due to improper design or manufacturing problems.*
- *Ink and markings in potted areas.*
- *Microphonic susceptibility.*
- *Device heating in encapsulated areas.*
- *Retroactive improvements.*

Design Checklist… 1

- *Is the design consistent with safe operation in both the operational and test regimes?*
- *What is the lifetime requirement including test time at full voltage?*
- *Are key design elements as simple as practical?*
- *Do key design elements use proven approaches and processes?*
- *Do the design and processes control voids and gaps?*
- *Have the critical spacing's been identified and analyzed to assure that all gradients are consistent with the unit lifetime requirement?*
- *Do high voltage joints use properly sized solder balls or other methods or controlling the local field gradient?*
- *Does the box venting design sized to be consistent with required pumpdown time constant?*

Design Checklist… 2

- *Is sleeving used or can wire insulation debond in a way that creates an insulation gap or void?*
- *Do the high voltage resistors or other components with applied high voltage have a hollow core that can break down?*
- *Are the encapsulated areas designed to allow for priming of bare metal and/or processing of the bare surfaces?*
- *Does the design incorporate a V/10 function or some other means of achieving safe test of both the HVPS and downstream circuitry?*
- *Are the design and test setups consistent with appropriate safety standards?*
- *Does the design employ effective arc suppression and protection that are consistent with the grounding approach.*
- *Is headroom and control range consistent with test margins?*

Progressive Development Process…

- *A high voltage system approach intended to achieve a high level of performance and reliability requires a progressive series of design and implementation steps to be fully successful.*
  - *Early and rapid **iterative process to develop optimal system requirements** through selective breadboarding and critical demonstrations.*
  - *Detailed design plan that documents the requirements and basis of both hardware and process qualification for each system element **including** the interface to the user.*
  - ***Functional Brassboard that allows early demonstration** of design and full quantitative understanding of elemental performance.*
  - *Life test Brassboard of EM that **allows early accelerated high voltage life verification**. **DO NOT TRY AND WRING OUT THE DESIGN ON THE EM UNIT!***
  - *EQM (if required).*
  - *PFM + FM + Spare Units tested according to a progressive **2 phase test strategy**.*

"T-E-M-P" Design Approach…

- *Successful execution of the careful and detailed "Thermal-Electrical-Mechanical-Process" approach for the integrated elements of your design will determine the success of its implementation.*
  - *Control the design from the top-down and end-to-end.*
  - *Synthesize your design as a system of familiar elements that deliver a deterministic result.*
  - *Manage all T-E-M-P interfaces **by design**.*
  - *Use rational design criteria for key resources.*
  - *Control performance and margins by design.*
  - *Use analysis to verify the design rather than a way to make problems disappear.*

Achieving Deterministic Performance… 1

- *Deterministic performance in our context means that the high voltage unit and associated system not only meets its requirements but is also fully understood and tested functionally down to the element level.*
- *Operational states in response to control inputs together with off-nominal states such as turn-on, turn-off and stand-by states should be predictable and have **known measured system responses that assure safe and reliable operation.***
- *The unit should be testable at the element level to verify that it **performs as designed** as part of a larger test program intended to verify that the system requirements are satisfied.*

Achieving Deterministic Performance… 2

- *Achieving deterministic performance starts with the establishing the key T-E-M-P design factors, executing the design, controlling manufacture and then executing a detailed adjustment and test program.*
  - *Design realism and robustness.*
  - *Design precision yielding repeatable measurements and trend metrics.*
  - *Proper selection and utilization of parts.*
  - *Functional partitioning.*
  - *E-Field management.*
  - *Control of systematic errors.*
  - *Tolerance to arcing and random factors.*
  - *Adjusting to the center of the distribution.*
  - *Functional stabilization.*

Designing for Manufacture… 1

- *Successful manufacture of a high voltage system starts with the use of controlled, inspectable processes for a design that has had its requirements aligned to the application of proven functional elements.*
  - *Use of proven processes consistent with required element and system performance and reliability.*
  - *Managed assembly flow using detailed procedures to minimize damage or contamination of key components during handling and cleaning.*
  - *Perform engineering supervision of all key process steps.*
  - *Define Engineering and Quality inspections at key process points.*
  - *Ensure processes are matched to assembly capability of organization.*
  - *Use a build sequence that allows for a 2-phase test strategy.*

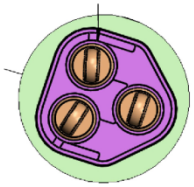
Examples of Detailed Process Control. Explain the WHY as well as the WHAT!

Designing for Manufacture… 2

Continued		Initials/Date	Inspect/Date	Extension
12	Install leaded TOP and BOT side passive components, test points and transistors EXCEPT FOR SAT components (shown in green on BOT side) R3, R125, R217, RN101, RN102, RN201, RN202, T101, T102, T201, T202, Q101, Q108, Q201, Q208, C131, C225, D105-D120, D124-D126, D205-D220 and D224-D227. *Note: some of the parts lay down on the board while other parts stand up. Take care to assure that parts that lay down have strain relief on leads.* *Note: Wire ends on C113, C116, C134, C170, C207, C210, C228, C270, D104, D105, D204, D205, R12, R134, R178, R21, R226 and R270 should be trimmed to less than .010 inches and reflowed to eliminate sharp points per procedure BE/999/96/032A.* *Note that C171, C172, C271, C272, R182-R184 and R282-R284 are not part of circuit board assembly and will be installed in the "ear" sections of the module later in this procedure.* If there are any other missing parts identify them below: _____ _____ _____ _____ _____ _____		XXXXX	
*N	Take care to protect and not contaminate parts installed in previous steps.			
13	Install Microcircuits on TOP side.		XXXXX	
14	Install heat shrink tubing on FB101, FB102, FB201 and FB202.		XXXXX	
15	Form leads of Q101, Q108, Q201 and Q208 by splaying out the base and collector leads to fit into the PC board. Maintain the emitter leads straight out of the parts.		XXXXX	
16	Slide ferrite beads on to the emitter leads of Q101, Q108, Q201 and Q208 and then insert the parts into the PC board such that the bead is still free to move with ~.010 inch clearance. Solder parts in place.		XXXXX	
17	Clean thoroughly with IPA or ethyl alcohol. *Unit should be handled with gloves from this point onward.*		XXXXX	
IP	*INSPECTION POINT- Complete parts placement, soldering inspection and lead length inspection. Also verify polarity of all tantalum capacitors.*	XXXXX		
N	*Note: Several of the steps below involve the installation of specialty items or high voltage parts with associated placement and lead trimming issues. They are to be performed under the supervision of S. Battel or with his cognizance*	XXXXX	XXXXX	XXXXX

Continued		Initials/Date	Inspect/Date	Extension
34	Using same (or another) batch of EN-11 from STEP 29, install top multiplier shields T100 (CIPS-M-24015) and T200 (CIPS-M-24016) . Cure for 16 hours at 60C (in parallel with STEP 29) prior to further handling.		XXXXX	
35	Under the direction of S. Battel, apply EN-11 per procedure BE/999/94/248A to bottom-side high voltage resistor shield CIPS-M24013 in RN101 and RN201 locations. Take care to achieve a void-free interface. Cure for 16 hours at 60C prior to further handling. MIX# _____		XXXX	
36	Using same (or another) batch of EN-11 from STEP 31, install bottom multiplier shields B100 (CIPS-M-24018) and B200 (CIPS-M-24017) . Cure for 16 hours at 60C (in parallel with STEP 31) prior to further handling.		XXXXX	
37	Pre-form leads of high voltage resistors RN101, RN102, RN201 and RN202 and install leaving .020 inch gap above insulators. Trim HV leads (1 place on each part) to eliminate sharp points and re-flow solder to minimize potential for HV breakdown per procedure BE/999/96/032A. Clean locally using IPA.		XXXXX	
38	Install thermistor R3. Clean locally using IPA.		XXXXX	
39	Mix Cab-O-Sil EN-11 per procedure BE/999/94/059B. Under the direction of S. Battel, stake RN101, RN102, RN201, RN202, C131, C225 and R3. Cure for 6 hours at room temperature followed by 16 hours at 60C prior to further handling.		XXXXX	
40	Prepare a 10 gram batch of Epo-Tek H22 silver epoxy per BE/999/98/115. Be sure to retain some of the material for a cure coupon. MIX# _____		XXXXX	
41	Form chassis stubs from STEP 22 with modest strain relief to be in contact with the center of the box wall. Apply epoxy to the wire and wall to effect a solid electrical connection. *Take great care to ensure that no silver epoxy touches the PC board or any high voltage insulators.*		XXXXX	
42	Insert 2 HV shields (PN BE21903740B1) into turrets and solder in place. Ensure that shields are installed flush with bottom of turrets and have good solder fillet.		XXXXX	
43	Clean thoroughly.		XXXXX	
44	Install T101, T102, T201 and T202 under the direction of S. Battel. Trim Pin 2 on each device per procedure BE/999/96/032A. *Note that once magnetics devices are installed, board cannot be immersed in solvents and must be very carefully cleaned to avoid attack and crazing of magnet wire. Take great care with all cleaning processes.*		XXXXX	

Designing for Manufacture… 3

Continued		Initials/Date	Inspect/Date	Extension
48	Fit connector and install jackposts and install hardware. **Note that the connector is back mounted.**		XXXXX	
49	Carefully route and cut the connector wires one by one and install them with appropriate strain relief to their individual pad locations. **Take care to route wires such that SAT components and test point are not covered or obscured.**		XXXXX	
IP	***INSPECTION POINT- Verify installation of connector and routing of wires.***	XXXXX		
50	Test fit Reynolds wire in Z-Feedthrus. Ream hole as required for snug sliding fit of wire. Clean parts after handling.		XXXXX	
51	Prepare a small batch of EC2850FT/Cat9 epoxy per BE/999/94061B. Be sure to retain some of the material for a cure coupon. MIX# _____		XXXXX	
52	Under direction of S. Battel, install pins in high voltage isolators aligned per the drawing below using EC2850FT. Ensure that pins are sealed to the isolators since the part will eventually be potted. 		XXXXX	
53	Under the direction of S. Battel, apply EN-11 per procedure BE/999/94/248A to each high voltage isolator assembly and the mating box surfaces inside high voltage pockets. Insert isolator and apply pressure to assure void-free wetting. Cure for 16 hours at 60C prior to further handling. MIX# _____		XXXX	
54	Using same batch of EN-11, wet Z-Feedthru mounting interfaces and install. Make sure close together holes are down toward the PC board. Cure for 16 hours at 60C prior to further handling.		XXXXX	
55	Test fit -100 (left side) and -200 (right side) filter boards in respective ears.		XXXXX	

Continued		Initials/Date	Inspect/Date	Extension
66	Prepare 6 Reynolds wires by trimming them to 7 inches in length.		XXXXX	
67	Under the direction of S. Battel, route the two MHV wires through their respective lower hole in each Z-Feedthru. Wires should route straight along PC board as shown on the assembly drawing. Terminate at each MHV feedthru pin respectively with hook-splice and ball solder joint. **Take care to retain stress relief in what will be the finally staked position.**		XXXXX	
68	Under the direction of S. Battel, route the two SHV wires through their respective middle hole in each Z-Feedthru. Wires should route around shield and along outer wall terminating at R184 and R284 respectively with hook-splice and ball solder joint. **Take care to retain stress relief in what will be the finally staked position.**		XXXXX	
69	Under the direction of S. Battel, route the two FHV wires through their respective upper hole in each Z-Feedthru. Wires should route around the multiplier shield in contact with it above the PC board. Terminate the wire at R182 and R282 respectively with hook-splice and ball solder joint. **Take care to retain stress relief and meet spacing requirement for 7000 volts in what will be final staked position.**		XXXXX	
70	Clean locally using IPA or ethyl alcohol.		XXXXX	
71	Under direction of S. Battel, position and stake high voltage wires using Cab-O-Sil filled EN-11 per BE/999/94/059B. Take care to ensure proper positioning of wires since high voltage breakdown can occur if not properly performed.		XXXXX	
72	Under direction of S. Battel, route and terminate the MHV and SHV wires at their respective PC board pads.		XXXXX	
73	Clean locally using IPA or ethyl alcohol.		XXXXX	
74 **N*	Under the direction of S. Battel, trim leads on 10 kV high voltage capacitors C131 and C225 to .7 inches. For ground lead of capacitors and lap solder to PC board. Clean locally using IPA. ***Proper thermal strain relief is very important. Ensure loop is ~.125 inches above PC board.***		XXXXX	
75	Under direction of S. Battel, install stand-up high voltage parts R125 and R217 attaching to the floating lead for C131 and C217 respectively. Note that source end of R125 and R217 originate on PC board and require processing per BE/999/96/032A. Form the lead to assist the attachment of the FHV wires in the following step.		XXXXX	
76	Under the direction of S. Battel, install FHV wires on the floating lead for C131 and C217 such that the joint also captures the lead for R125 and R217 from the previous step. Solder with a very carefully done ball joint at a controlled height that maintains maximum spacing below the cover.		XXXX	

Designing for Analysis…

- *Designs should be functionally partitioned and incorporate test points such that each element can be functionally tested and then correlated with **key** analysis results.*
  - *Analysis should be performed at the system level as part of an integrated T-E-M-P strategy.*
  - *Precision designs should use components with inherent precision and stability or incorporate trim adjustments that center unit performance at the preferred mid-point of the functional and/or aging distribution.*
  - *Most elements once incorporated into a high voltage system are best tested for overall robustness through a VTF approach where every internal element is parametrically monitored and trended.*
- *If possible, high voltage elements should be designed with symmetry and controlled geometries that are understandable through hand analysis as well as computer-aided techniques.*

Designing for Test… 1

- *High voltage designs are best understood through detailed functional testing at both the element and system level.*
  - *Ability to test each element through its full design range.*
  - *Simple and controlled interfaces.*
  - *Partitioning and insertion of accessible test points.*
  - *Compatible with standard and reproducible test setups.*
  - *Precision necessary for repeatable tests and repeatable metrics.*
- *Build in the capability to test in 2 phases.*
  - ***Phase 1 testing to design** at the element level (typically prior to irreversible steps such as potting) **using internal test points**, wide temperature/stress margins and incremental temperature steps.*
  - ***Phase 2 testing to unit requirements** after unit closeout over a narrower range using **correlated internal monitors**.*

Designing for Test... 2

Comparison of In-Process Test and Final Bench Test Data Sets

JAN 09 2012

IUVS HVPS TEMP TEST DATA SHEET UNIT Fm-02 SN -02 DATE:

TEST CONDITION: +20/+17 MEASURED TEMP: +19.7 TIME: 1038

MVHDACSET→ PARAMETER	+/-15 VOLTS NOM LOAD 0.000	1.000	2.000	3.000	4.000	5.000
TEMPMON (CH105)	12.34 K	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
HV OFF	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_A	4.81 /-1.85	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_B	4.82 /-1.84	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
FHV_A/B_ON	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_A	23.37 /-1.83	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_B	23.05 /-1.82	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
MHV+FHV_A/B_ON	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I_A	28.91	30.90	33.68	36.38	38.2	42.0
-15I_A	-1.94	XXXXX	XXXXX	XXXXX	XXXXX	-1.88
MFREQ_A	66.407	67.675	68.256	68.715	68.528	69.073
FFREQ_A	59.177	XXXXX	XXXXX	XXXXX	XXXXX	59.111
+GATE_A (CH221)	36.6	XXXXX	XXXXX	XXXXX	XXXXX	33.4
-GATE_A (CH221)	-198.7	XXXXX	XXXXX	XXXXX	XXXXX	-198.5
MHV_A (CH222)	70.4	198.1	397.4	596.5	755.9	595.3
FHV_A (CH223)	6074	6202	6402	6602	6802	7002
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I_B	28.42	30.90	33.17	35.83	38.5	41.1
-15I_B	-1.93	XXXXX	XXXXX	XXXXX	XXXXX	-1.88
MFREQ_B	66.952	68.264	68.854	69.322	69.537	69.892
FFREQ_B	58.762	XXXXX	XXXXX	XXXXX	XXXXX	58.693
+GATE_B (CH224)	38.0	XXXXX	XXXXX	XXXXX	XXXXX	38.0
-GATE_B (CH224)	-194.2	XXXXX	XXXXX	XXXXX	XXXXX	-197.8
MHV_B (CH225)	69.8	198.1	397.4	596.4	755.8	955.3
FHV_B (CH226)	6073	6202	6402	6602	6802	7002
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
DACINPUT_A (CH111)	0.000	1.000	XXXXX	2.599	XXXXX	4.999
MHVMON_A (CH112)	0.200	0.560	XXXXX	1.681	XXXXX	2.804
FHVMON_A (CH113)	2.431	2.483	XXXXX	2.643	XXXXX	2.803
DACINPUT_B (CH114)	0.000	1.000	XXXXX	2.588	XXXXX	4.998
MHVMON_B (CH115)	0.199	0.560	XXXXX	1.681	XXXXX	2.804
FHVMON_B (CH116)	2.434	2.487	XXXXX	2.648	XXXXX	2.808
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
GATE50_A (CH201)	55.558	55.590	XXXXX	XXXXX	XXXXX	55.478
GATE50_B (CH202)	55.634	55.615	XXXXX	XXXXX	XXXXX	55.538
VDAC_A (CH203)	0.000	0.599	XXXXX	XXXXX	XXXXX	4.998
MSENSE_A (CH204)	0.257	0.998	XXXXX	XXXXX	XXXXX	5.002
FSENSE_A (CH205)	6.078	6.207	XXXXX	XXXXX	XXXXX	9.007
DSENSE_A (CH206)	3.338	3.328	XXXXX	XXXXX	XXXXX	3.328
MERROR_A (CH207)	1.267	1.415	XXXXX	XXXXX	XXXXX	2.242
FERROR_A (CH208)	2.985	3.000	XXXXX	XXXXX	XXXXX	3.092
DIODEREF_A (CH209)	-6.328	-6.328	XXXXX	XXXXX	XXXXX	-6.327
VDAC_B (CH210)	0.000	0.598	XXXXX	XXXXX	XXXXX	4.998
MSENSE_B (CH211)	0.254	0.859	XXXXX	XXXXX	XXXXX	5.005
FSENSE_B (CH212)	6.038	6.243	XXXXX	XXXXX	XXXXX	9.008
DSENSE_B (CH213)	3.337	3.327	XXXXX	XXXXX	XXXXX	3.327
MERROR_B (CH214)	1.245	1.394	XXXXX	XXXXX	XXXXX	2.167
FERROR_B (CH215)	2.941	2.955	XXXXX	XXXXX	XXXXX	2.946
DIODEREF_B (CH216)	-6.322	-6.322	XXXXX	XXXXX	XXXXX	-6.322

A4-1.2

JAN 22 2012

IUVS HVPS BENCH TEST DATA SHEET UNIT Fm-02 SN -02 DATE:

TEST CONDITION: AMBIENT MEASURED TEMP: 68F TIME: 1108

MHVDACSET→ PARAMETER	+/-15 VOLTS NOM LOAD 0.000	1.000	2.000	3.000	4.000	5.000
TEMPMON (CH105)	10.07K	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
HV OFF	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_A	4.82/-1.85	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_B	4.82 /-1.83	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
FHV_A/B_ON	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_A	23.87/-1.84	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_B	23.54/-1.83	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
MHV+FHV_A/B_ON	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I_A	29.46	31.52	34.40	37.17	39.8	42.7
-15I_A	-1.95	-1.93	-1.91	-1.91	-1.91	-1.90
+GATE_A (CH221)	38.6	XXXXX	XXXXX	XXXXX	XXXXX	38.6
-GATE_A (CH221)	-198.6	XXXXX	XXXXX	XXXXX	XXXXX	-200.0
MHV_A (CH222)	69.4	189.9	388.3	587.4	756.8	956.4
FHV_A (CH223)	6072	6202	6402	6602	6802	7002
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I_B	28.95	31.00	33.84	36.58	38.3	42.0
-15I_B	-1.94	-1.91	-1.90	-1.89	-1.89	-1.89
+GATE_B (CH224)	38.0	XXXXX	XXXXX	XXXXX	XXXXX	38.1
-GATE_B (CH224)	-193.8	XXXXX	XXXXX	XXXXX	XXXXX	-194.3
MHV_B (CH225)	68.8	199.0	388.2	587.3	756.8	956.4
FHV_B (CH226)	6073	6203	6403	6603	6803	7004
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
DACINPUT_A (CH111)	0.000	1.000	2.000	2.998	3.998	4.999
MHVMON_A (CH112)	0.195	0.560	1.120	1.681	2.242	2.804
FHVMON_A (CH113)	2.430	2.482	2.562	2.642	2.722	2.802
DACINPUT_B (CH114)	0.000	1.000	2.000	2.998	3.999	4.999
MHVMON_B (CH115)	0.193	0.560	1.121	1.681	2.243	2.805
FHVMON_B (CH116)	2.434	2.487	2.567	2.647	2.727	2.808

A6-1.2

Designing for Test… 3

Unit Comparisons from Different Builds 7 years Apart

IUVS HVPS TEMP TEST DATA SHEET UNIT FM-02 SN -02 DATE: JAN 09 2012

TEST CONDITION: +20/RT MEASURED TEMP: +19.7 TIME: 1038

+/-15 VOLTS NOM LOAD

MVHDACSET→ PARAMETER	0.000	1.000	2.000	3.000	4.000	5.000
TEMPMON (CH105)	12.34 K	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
HV OFF	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_A	4.81 /-1.85	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_B	4.82 /-1.84	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
FHV_A/B_ON	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_A	27.37 /-1.83	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_B	27.05 /-1.82	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
MHV+FHV_A/B_ON	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I_A	28.91	30.90	33.68	36.38	38.2	42.0
-15I_A	-1.94	XXXXX	XXXXX	XXXXX	XXXXX	-1.89
MFREQ_A	66.407	67.675	68.256	68.715	68.528	69.073
FFREQ_A	59.177	XXXXX	XXXXX	XXXXX	XXXXX	59.111
+GATE_A (CH221)	36.6	XXXXX	XXXXX	XXXXX	XXXXX	33.4
-GATE_A (CH221)	-198.7	XXXXX	XXXXX	XXXXX	XXXXX	-199.5
MHV_A (CH222)	70.4	198.1	397.4	596.5	755.9	995.3
FHV_A (CH223)	6074	6202	6402	6602	6802	7002
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I_B	28.42	30.40	32.17	35.83	38.5	41.1
-15I_B	-1.93	XXXXX	XXXXX	XXXXX	XXXXX	-1.88
MFREQ_B	66.952	68.264	68.854	69.322	69.537	69.892
FFREQ_B	58.762	XXXXX	XXXXX	XXXXX	XXXXX	58.693
+GATE_B (CH224)	[illegible]	XXXXX	XXXXX	XXXXX	XXXXX	38.0
-GATE_B (CH224)	-194.2	XXXXX	XXXXX	XXXXX	XXXXX	-197.8
MHV_B (CH225)	[illegible]	198.1	397.4	596.4	795.8	995.3
FHV_B (CH226)	6073	6202	6402	6602	6802	7002
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
DACINPUT_A (CH111)	0.000	1.000	XXXXX	2.559	XXXXX	4.995
MHVMON_A (CH112)	0.200	0.560	XXXXX	1.681	XXXXX	2.804
FHVMON_A (CH113)	2.431	2.483	XXXXX	2.643	XXXXX	2.803
DACINPUT_B (CH114)	0.000	1.000	XXXXX	2.588	XXXXX	4.998
MHVMON_B (CH115)	0.199	0.560	XXXXX	1.681	XXXXX	2.804
FHVMON_B (CH116)	2.436	2.483	XXXXX	2.648	XXXXX	2.808
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
GATE50_A (CH201)	55.558	55.540	XXXXX	XXXXX	XXXXX	55.478
GATE50_B (CH202)	55.634	55.615	XXXXX	XXXXX	XXXXX	55.538
VDAC_A (CH203)	0.000	0.599	XXXXX	XXXXX	XXXXX	4.998
MSENSE_A (CH204)	0.257	0.918	XXXXX	XXXXX	XXXXX	5.002
FSENSE_A (CH205)	6.078	6.247	XXXXX	XXXXX	XXXXX	9.004
DSENSE_A (CH206)	3.338	3.328	XXXXX	XXXXX	XXXXX	3.328
MERROR_A (CH207)	1.267	1.415	XXXXX	XXXXX	XXXXX	2.242
FERROR_A (CH208)	2.785	3.000	XXXXX	XXXXX	XXXXX	3.092
DIODEREF_A (CH209)	-6.328	-6.328	XXXXX	XXXXX	XXXXX	-6.327
VDAC_B (CH210)	0.000	0.598	XXXXX	XXXXX	XXXXX	4.998
MSENSE_B (CH211)	0.254	0.859	XXXXX	XXXXX	XXXXX	5.005
FSENSE_B (CH212)	6.038	6.243	XXXXX	XXXXX	XXXXX	7.008
DSENSE_B (CH213)	3.337	3.327	XXXXX	XXXXX	XXXXX	3.327
MERROR_B (CH214)	1.245	1.394	XXXXX	XXXXX	XXXXX	2.167
FERROR_B (CH215)	2.541	2.555	XXXXX	XXXXX	XXXXX	3.040
DIODEREF_B (CH216)	-6.322	-6.322	XXXXX	XXXXX	XXXXX	-6.322

Δ4-1.2

AIM HVPS TEMP TEST DATA SHEET UNIT 1F SN 004ND DATE: 12/16/04 Δ4-1.1b

TEST CONDITION: +20C MEASURED TEMP: +19.3 TIME: 0936

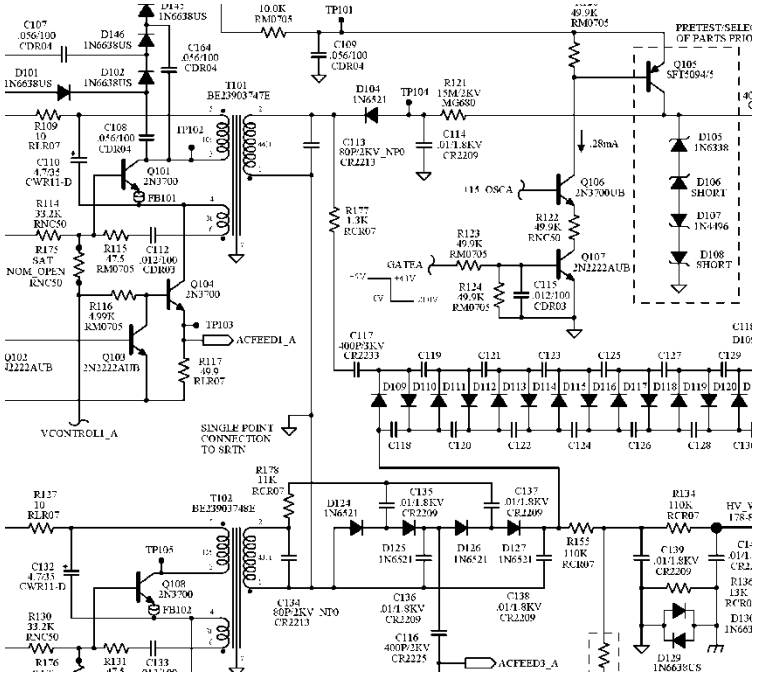
+/-15 VOLTS NOM LOAD

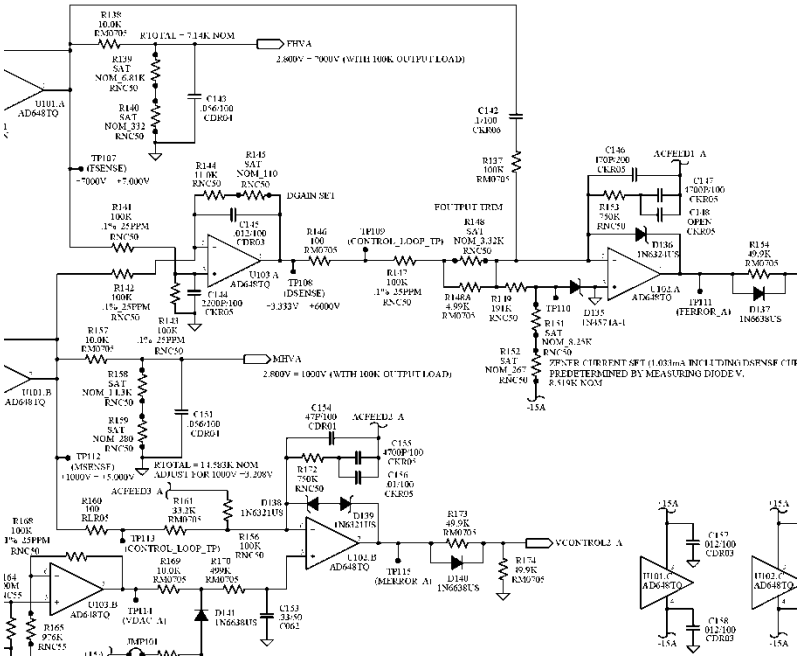
MVHDACSET→ PARAMETER	0.000	1.000	2.000	3.000	4.000	5.000
TEMPMON (CH105)	11.727	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
HV OFF	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_A	5.00 /-2.03	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_B	5.03 /-1.98	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
FHV_A/B_ON	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_A	28.32 /-2.00	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I/-15I_B	28.16 /-1.96	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
MHV+FHV_A/B_ON	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I_A	29.64	31.89	34.56	37.10	39.5	42.0
-15I_A	-2.01	XXXXX	XXXXX	XXXXX	XXXXX	-1.91
MFREQ_A	67.784	68.559	69.610	69.937	70.127	70.230
FFREQ_A	60.527	XXXXX	XXXXX	XXXXX	XXXXX	60.755
+GATE_A (CH221)	39.1	XXXXX	XXXXX	XXXXX	XXXXX	35.1
-GATE_A (CH221)	-200.4	XXXXX	XXXXX	XXXXX	XXXXX	-200.3
MHV_A (CH222)	70.1	198.1	398.4	597.4	796.6	995.8
FHV_A (CH223)	6071.3	6201.2	6401.1	6600.6	6800.4	7000.2
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
+15I_B	29.38	31.46	34.11	36.62	39.1	41.6
-15I_B	-1.97	XXXXX	XXXXX	XXXXX	XXXXX	-1.88
MFREQ_B	67.003	68.191	68.814	69.129	69.305	69.412
FFREQ_B	60.367	XXXXX	XXXXX	XXXXX	XXXXX	60.210
+GATE_B (CH224)	39.0	XXXXX	XXXXX	XXXXX	XXXXX	39.3
-GATE_B (CH224)	-202.2	XXXXX	XXXXX	XXXXX	XXXXX	-202.3
MHV_B (CH225)	69.9	198.2	398.6	597.7	797.1	996.5
FHV_B (CH226)	6072.9	6202.3	6401.9	6601.3	6801.0	7000.7
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
DACINPUT_A (CH111)	0.0000	1.0058	XXXXX	2.5555	XXXXX	4.9955
MHVMON_A (CH112)	.197	.560	XXXXX	1.680	XXXXX	2.802
FHVMON_A (CH113)	2.427	2.477	XXXXX	2.638	XXXXX	2.853
DACINPUT_B (CH114)	0.0000	.9998	XXXXX	2.5955	XXXXX	4.9955
MHVMON_B (CH115)	.197	.560	XXXXX	1.681	XXXXX	2.803
FHVMON_B (CH116)	2.428	2.480	XXXXX	2.638	XXXXX	2.859
XXXXXXXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
GATE50_A (CH201)	55.500	55.482	XXXXX	XXXXX	XXXXX	55.415
GATE50_B (CH202)	55.487	55.468	XXXXX	XXXXX	XXXXX	55.355
VDAC_A (CH203)	-.0098	.9992	XXXXX	XXXXX	XXXXX	4.9987
MSENSE_A (CH204)	1.3126	.9996	XXXXX	XXXXX	XXXXX	Comm.0
FSENSE_A (CH205)	6.0795	6.2085	XXXXX	XXXXX	XXXXX	7.4092
DSENSE_A (CH206)	3.337	3.333	XXXXX	XXXXX	XXXXX	3.327
MERROR_A (CH207)	1.226	1.355	XXXXX	XXXXX	XXXXX	2.088
FERROR_A (CH208)	3.113	3.142	XXXXX	XXXXX	XXXXX	3.244
DIODEREF_A (CH209)	-6.28833	-6.28538	XXXXX	XXXXX	XXXXX	-6.28644
VDAC_B (CH210)	-.0008	.9993	XXXXX	XXXXX	XXXXX	4.9952
MSENSE_B (CH211)	.3511	.9997	XXXXX	XXXXX	XXXXX	Comm.0
FSENSE_B (CH212)	6.0619	6.2716	XXXXX	XXXXX	XXXXX	7.0114
DSENSE_B (CH213)	3.333	3.327	XXXXX	XXXXX	XXXXX	3.283
MERROR_B (CH214)	1.220	1.258	XXXXX	XXXXX	XXXXX	2.111
FERROR_B (CH215)	3.091	3.065	XXXXX	XXXXX	XXXXX	3.180
DIODEREF_B (CH216)	-6.24021	-6.24025	XXXXX	XXXXX	XXXXX	-6.24025

Designing for Test... 4

Test points should be placed to allow for easy measurement and to give full insight into design performance.

Example Test Point Placement





Designing for Repair…

- *Once specialty coatings are applied or encapsulation occurs, most high voltage elements cannot be repaired with guaranteed reliability.*
  - *Insulation is materially degraded by the repair process.*
  - *Transitional boundaries or gaps introduced.*
- *Some elements such as magnetics can be replaced if the design is made compatible.*
- *Best approach is 2 phase testing with burn-in **prior** to final irreversible coating and encapsulation steps.*
  - *Also allows for higher temperature operation during process.*
- *Sparing philosophy must account for unit replacement including long processing time.*

We are "poachers"… fortunately poaching is legal in our business!

What Drives Technology in Our Business?

Electric Power Industry – *Largely overseas; Interests are ultra-high voltage techniques buried cable insulation performance and aging, insulator design, ceramic materials, modeling methods, measurement equipment, specialty fuel cell materials, nano-materials and diagnostic test methods.*

Automobile Industry – *Domestic and overseas; Interests are engineering plastics, power electronics, high temperature durability and material aging.*

Commercial Displays – *Largely overseas; Interests are transformer technology including piezo transformers and semiconducting coatings.*

Particle Accelerators – *Domestic but transitioning to overseas; Special interests are radiation effects on materials, analysis software, insulator design, high power DC and RF methods and pulse forming technology.*

RF and Microwave – *Domestic; Special interests in unique materials, high thermal conductivity materials, low dielectric constant materials, cables and connectors, specialty plating and coatings.*

Key High Voltage Components and Technologies…

- *Magnetic Devices*
- *Capacitors*
- *Diodes*
- *Resistors*
- *Specialty Opto-Couplers (Modulators)*
- *Shielded and Unshielded Cables*
- *Connectors/Terminations*
- *Materials and Coatings*
- *Analysis Software*

Game Changers…

Change comes slow but does come in our business!

- *Understanding of aging effects in dielectrics (1960's).*
- *Floating plate ceramic capacitors (1970's).*
- *High performance high voltage cables (1970's).*
- *HV601-801 (and similar devices) opto-modulators (1980's).*
- *Parylene coating technology (1990's).*
- *Fine-line precision high voltage resistors (1990's).*
- *3D Field Analysis tools (1990's).*
- *Nano-particles (almost there).*
- *Piezo transformers (almost there).*
- *Silicon Carbide parts (almost there)*
- *Diamond based materials (almost there)*

Eroding National Capabilities…

- *PC Board Manufacturing*
- *Plating and Coatings*
- *Specialty Magnetic Components*
- *Low Frequency Semiconductor Devices*
- *High Voltage Bipolar Transistors*
- *Non-RoHS Electronic Components*
- *Skilled Hand Assembly*

Develop Trust and Confidence in Your Key Vendors…

- *The key vendors I usually work with are the following although there are many others that are qualified as well.*
- ***CalRamic** (30+ years including KD)*
- ***VMI** (30+ years)*
- ***Reynolds** (30+ years)*
- ***Caddock** (30+ years)*
- ***SSDI** (20+ years)*
- ***Ohmcraft** (15+ years)*
- ***RJR** (15+ years)*
- ***Micropac** (10+ years)*

Don't be afraid to work with your vendors on special technology or component challenges!

Part Selection and Specification…

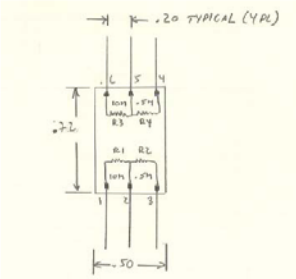
- *Don't be afraid to design a special part if it is inside your experience and if it results in a substantial simplification of the design or if it results in a substantial process or reliability improvement.*
- *Use SCD's or detailed spec sheets for parts and materials where element performance or reliability is critically dependent on fit or function. One great benefit of an SCD is that it reflects design intent and does not go out of date!*
- *Make sure your vendor is familiar with the key parameters that your design is dependent upon. Also work with your vendor on accepting parts if they are simply marginal on an uncritical but controlled parameter.*
- *Evaluate engineering devices out of same lot in parallel with screening and qualification to validate compatibility with design.*
- *Buy enough special parts to allow "cherry picking" for key parameters.*

SCD's Provide Clear Direction for Process Critical Parts… 1

Manufacturer's Part Number: CN-827

Quantity: 60 Delivered (plus TBD parts for testing/qualification at vendor). Note that extra parts are required to allow for selection in specific applications.

Body Size: 0.50" L X .72" H X .05 (max)" T



Resistance Ratio: 2 times 20:1

Value: 2 times 10.50 Megohms Overall; 10.0 Megohms/0.50 Megohm

Voltage Rating: 2,000 Vdc

Material Type: Flat 0.025" thick alumina substrate with non-inductive metal oxide resistance film on one side only. Dual resistor networks are mirror images of each other on opposing edges of substrate.

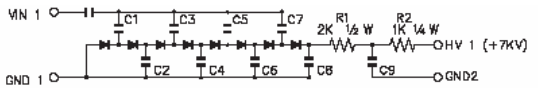
Coating: Blue Film over resistor pattern.

Ratio Tolerance: +/- 1.0%

Absolute Tolerance: +/- 1.0%

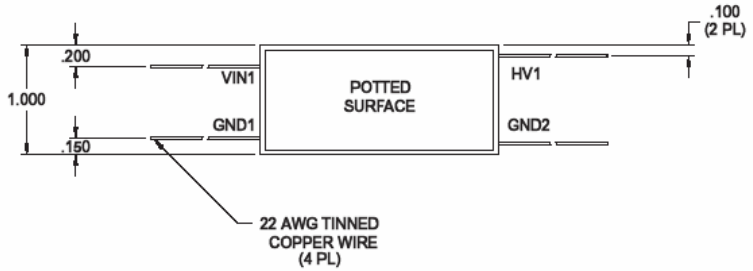
GND1,GND2 VIN, HV1

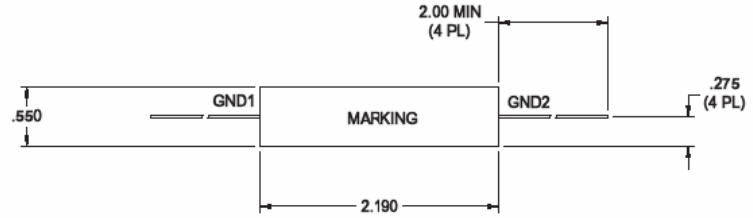
TOLERANCE
.XX ±.015
.XXX ±.010



NOTE:
1) SANDBLAST ALL SURFACES OF SHELL PRIOR TO ASSEMBLY.

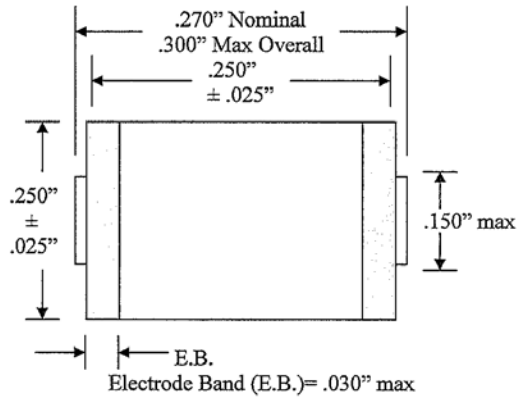
2) UNITS SHALL BE OVERPOTTED AND THEN THE TOP SURFACE GROUND TO THE FINISHED DIMENSION.

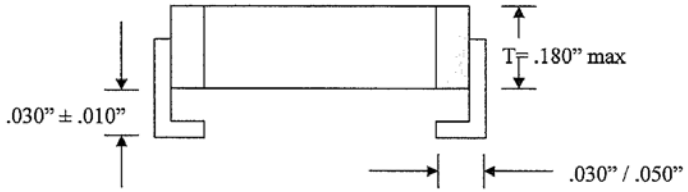




SCD's Provide Clear Direction for Process Critical Parts… 2

	Date	Initials	Comments
Rev.	3/24/03		
Rev.	3/28/03		P/N
Rev.			





1. Tab configuration= 'B' as shown
2. Tab material 0.009" phosphorous bronze with 300 µ in. min. 90% tin, 10% Lead (min)
3. High temp solder 10/88/2

Specifications

- Capacitance= 10,000 pF ± 10%
- Dissipation Factor= .025 max
- Insulation Resistance
  - 100,000 megΩ or 1000 megΩ–µF whichever is less @ 25°C
  - 10,000 megΩ or 100 megΩ-µF whichever is less @ 25°C
- Rated Voltage= 1800 VDC
- Dielectric Type= X7R (BR), -40% max @ -55°C to 125°C w/ rated voltage applied, 125 V/mil max
- C-SAM Testing 100% per CalRamic Drawing #10107 Rev A
- Group A testing IAW Mil-Prf-49467B, except voltage conditioning to be 240 hours min @ rated voltage.
- Voltage conditioning to be performed in flourinert or equivalent.
- Partial discharge testing 100 % per Mil-Prf-49467, 42% of DC rating, 100 picocoulombs max continuous.

Engineering Evaluation Methods…

- *Rapid evaluation of engineering parts or sample devices is an essential step prior to a final design commitment.*
- *A realistic "test as you operate" approach in combination with accelerated life testing and progressive "spiral" thermal testing can yield early confidence using relatively few parts and with a modest investment of time.*
- *Spiral tests typically involve 50 to 100 thermal cycles with a device operating in a realistic mode. Temperature range is progressively increased after each 10 to 20 cycles up to the device limits or to both understand device parametric performance and to determine the device limits.*

  Example: -10 to +40; -25 to +55; -40 to +70; -55 to +85…

Introducing Jeff Day to Discuss the Design and Proper Application of High Voltage Capacitors

CalRamic Technologies LLC

Jeff M. Day

President

jday@calramic.com

High Voltage Ceramic Capacitors

500 VDC – 20,000 VDC

2012 NASA/NESC
High Voltage Power Supply Design Workshop

April 2-3, 2012

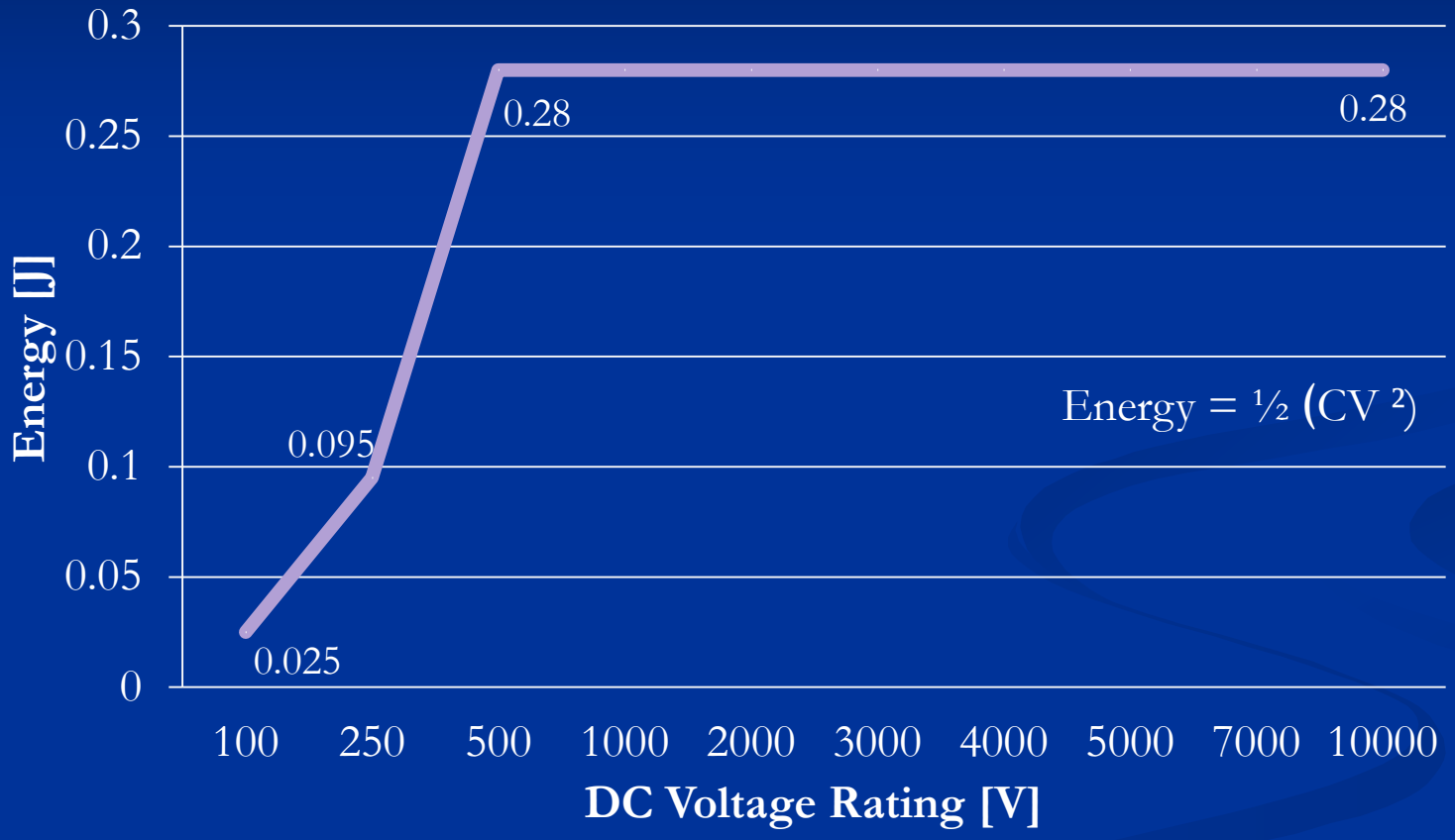
Topics

- High Voltage Dielectric Characteristics
- High Voltage Design Philosophies
- High Voltage Testing & Screening options

Our Philosophy of Reliability

- Materials Choice – High Quality, Consistent & Reliable Sources
- Space Quality HV Design Guidelines & Discipline
- Test & Screen to assure the first two are done well
- Establish a client/supplier partnership based on open communication to build trust & confidence

High Voltage Definition (X7R) Based Ceramics
Energy vs. Voltage Rating



High Voltage Ceramic Dielectric Types vs. Dielectric Constant

Dielectric Type	Dielectric Constant (K)
Ceramic	20 – 20,000
High Voltage Ceramic	K75 – 110 (NPO) K2000-2600(X7R)
Mica	4 – 8
Electrolytic Dry & Wet	4 – 10
Film	10
Paper	4 – 6
Porcelain	3 – 10
Tantalum Oxide	30 – 50
Glass	3 – 19
Air	1
Al_2O_3	9

- Two Conductive Layers
- Separated by a Dielectric Medium
- Ceramic exhibits much greater dielectric constants than the others, thereby offering a reduction geometries and mass
- As with any dielectric, understanding the limits of the material under load conditions in the application is critical

High Voltage Ceramic Dielectric Parameter Considerations

- Increases in K (Dielectric Constant) represent larger changes in intrinsic properties of the dielectric, such as:
  - Temperature Coefficient, Increases with higher K
  - **Voltage Coefficient, Increases with higher K**
  - Dissipation Factor, Increases with higher K
  - Dielectric Strength, Decreases with higher K's
  - Insulation Resistance, Decreases with higher K's
  - **Piezoelectric Properties increase with higher K's**
  - C-V Values, directly proportional to K

Voltage Temperature Coefficient (VTC) Summary

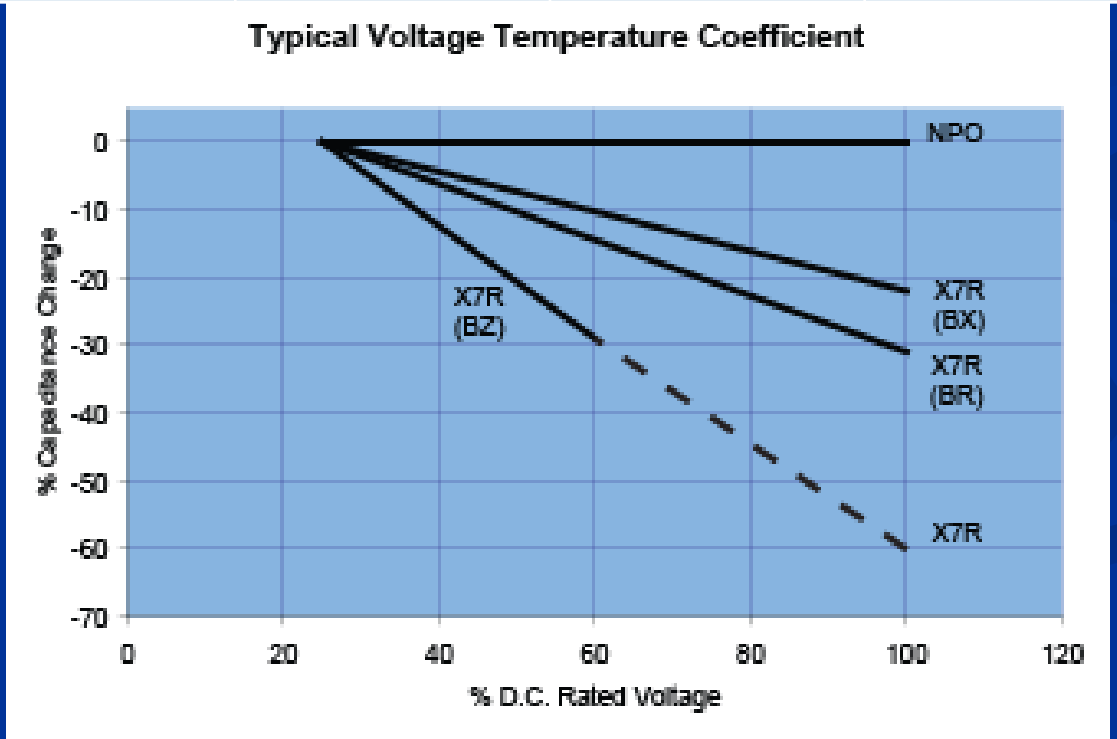
- Voltage Coefficient is based on material type and dielectric stress, as dielectric stress increases, voltage coefficient increases to a higher percentage of capacitance loss
- Power supply design considerations should be made based on the determination of the resulting capacitance at operating voltage & temperature

Voltage Temperature Coefficient

Change in Capacitance with Applied Voltage & Temperature

Ref: MIL-PRF-49467C

	Dielectric Type (EIA Designation)				
Specifications	NPO (H.V.)	X7R (MIL-COMM)	X7R-BX (L.V)	X7R-BR (H.V)	X7R-BZ (H.V)
Voltage Coefficient	**0**	**-70% Max**	**-25% Max**	**-40% Max**	**-40% Max @ 60% of Rated Voltage**



Ferroelectric and Prezoelectric Properties

- Ferroelectric Dielectric – The spontaneous alignment of electric dipoles in the ceramic with an applied field

  * X7R, $BaTiO_3$ Based Materials are Ferroelectric

  * NPO Material is not

- Piezoelectric Dielectrics – Due to the Ferroelectric nature of the dielectric, an applied field creates a mechanical distortion

- Care should be taken when using X7R based dielectrics in AC, or pulse DC conditions. NPO dielectrics can be used in a variety of applications due to their non-ferroelectric/piezoelectric nature

Ferroelectric Dielectrics

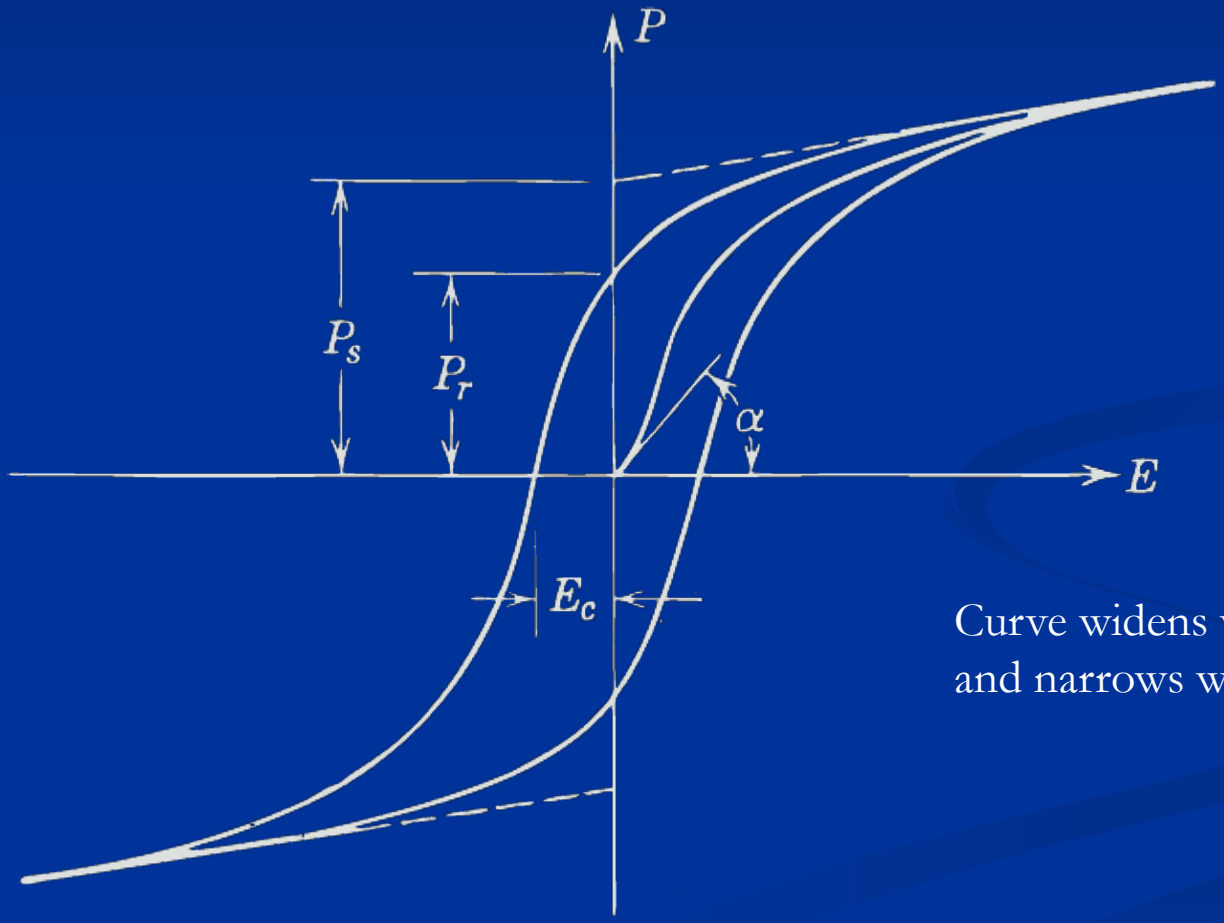
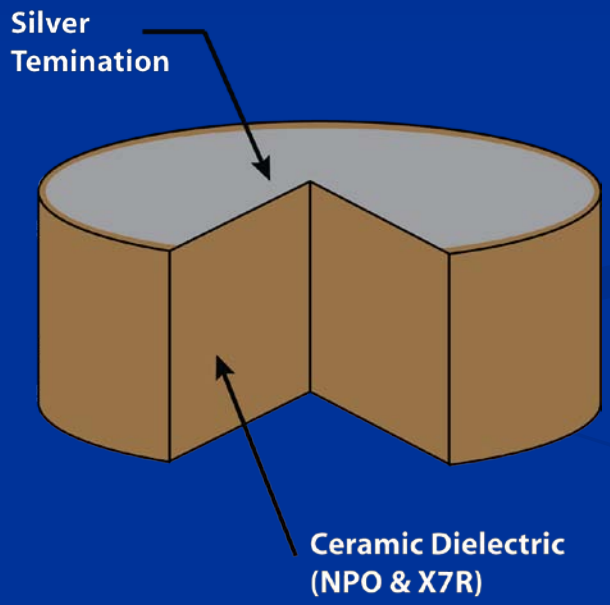


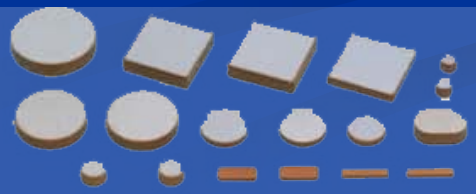
Fig. 18.32. A typical ferroelectric hysteresis loop
*J. Am. Chem. Soc., 58, 1486 (1936)

Curve widens with lower temperature, and narrows with higher temperature

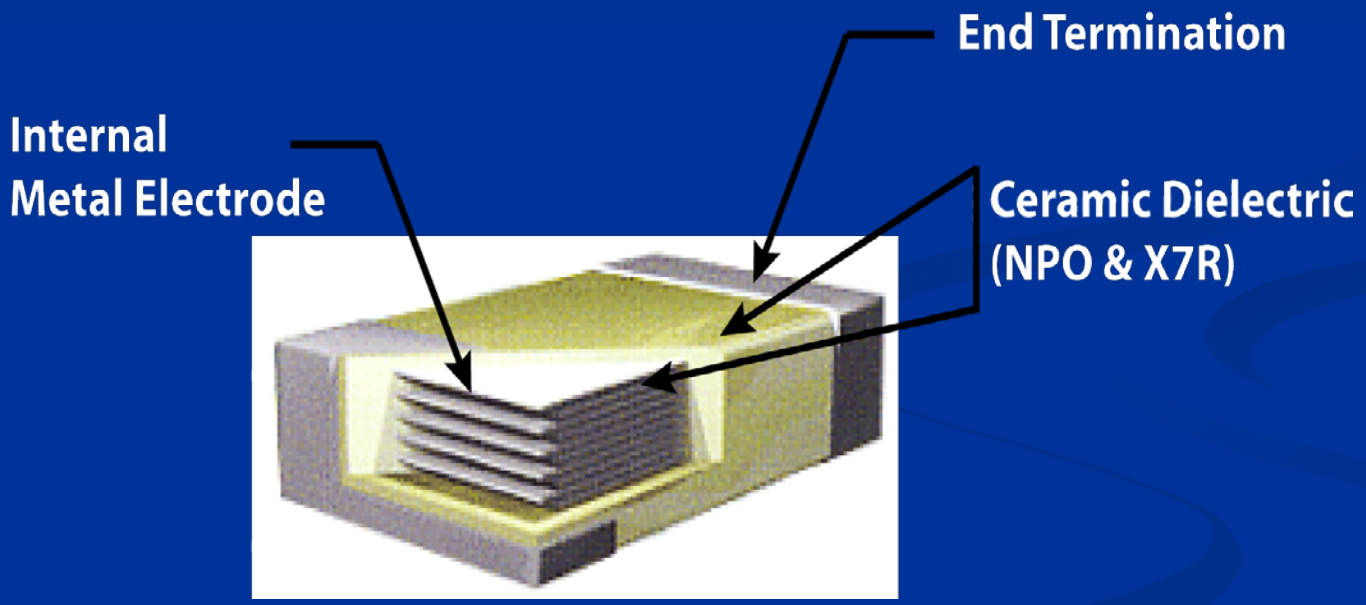
Design Philosophies

Typical Single Layer Ceramic Capacitor *(3,000VDC – 20,000VDC)*



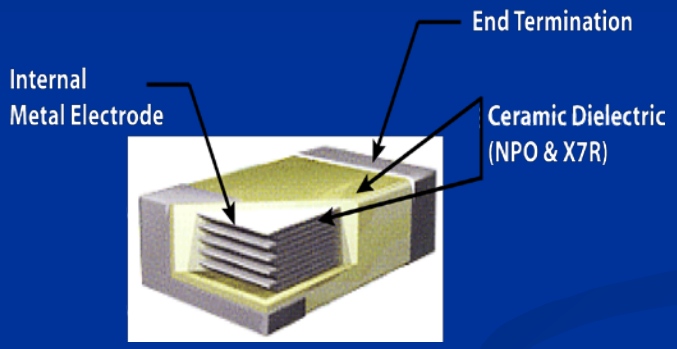


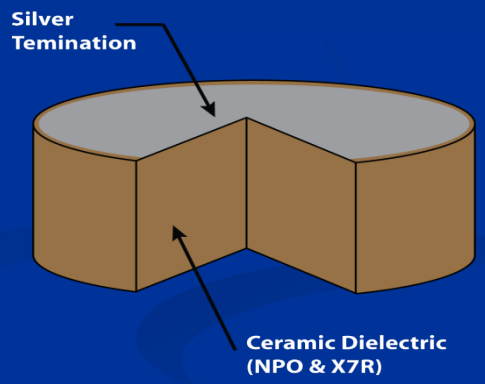
Typical Multilayer Ceramic Chip Capacitor *(500VDC – 10,000VDC)*



Formula for Calculating Capacitance of a Capacitor

$$\text{Capacitance} = \frac{.224 * K * A_f * N}{t_f}$$





Where: .224 = Constant

K = Dielectric Constant

A_f = Active Area

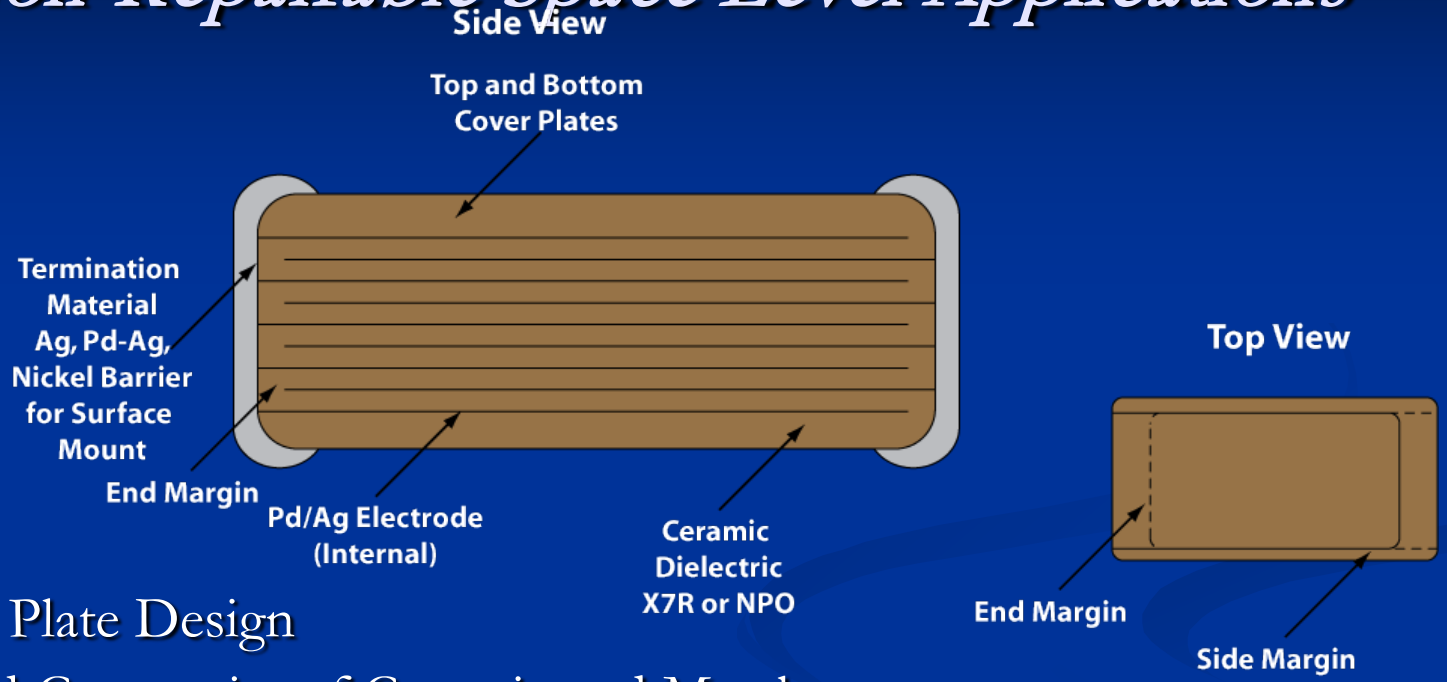
N = Number of Electrode Plates

t_f = Dielectric Thickness

Internal Construction

500 VDC – 1,000 VDC

Non-Repairable Space Level Applications

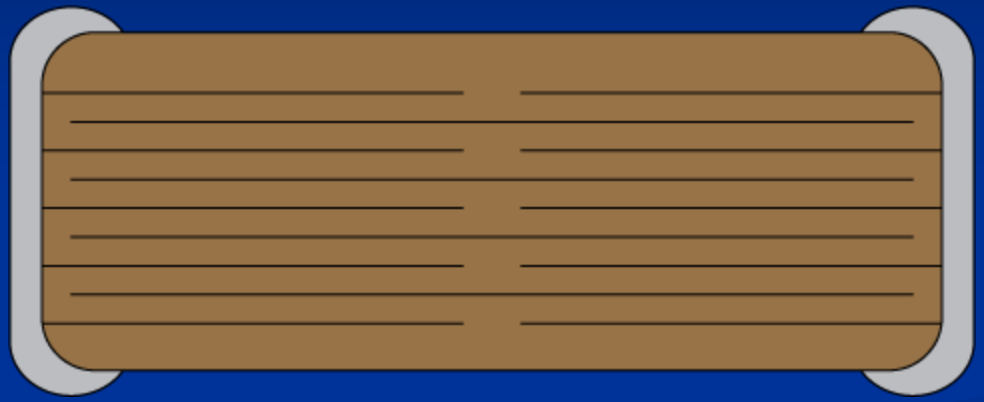


- Parallel Plate Design
- Co-fired Composite of Ceramic and Metal
- Design Considerations for Reliability
  - Dielectric Thickness < 125 volts/mil (X7R), 375 volts/mil (NPO)
  - Cover Plate Thickness at > 1.3x of Dielectric Thickness
  - End and Side Margins < 75 volts/mil
  - Radius on corners of electrode plates and external edges of structure

Internal Construction

2,000 VDC – 3,000 VDC

Non-Repairable Space Level Applications

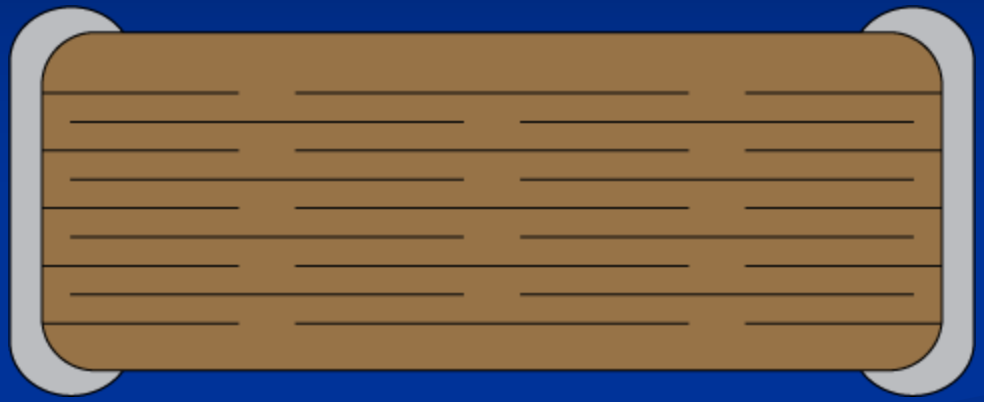


- Series Parallel Design
- Single Floating Plate
- 2 Capacitors in Series
- Reduction of Margin Stresses
- Same volts/mil Design Principles Apply

Internal Construction

4,000 VDC – 7,000 VDC

Non-Repairable Space Level Applications

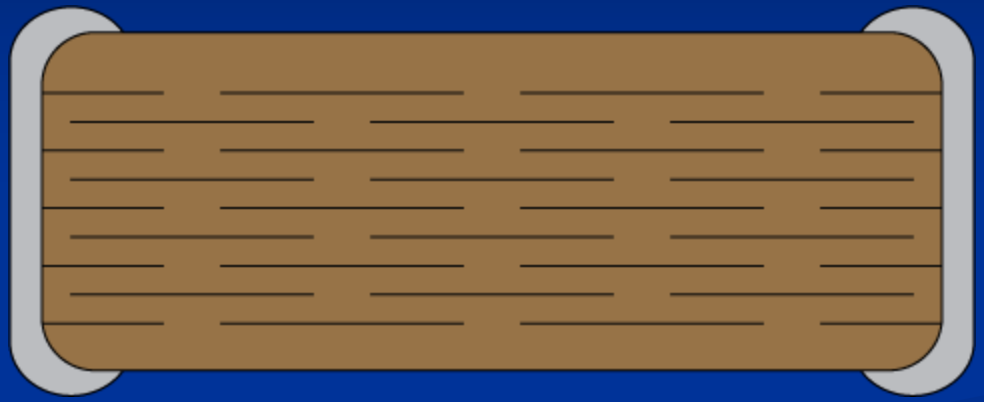


- Series Parallel Design
- 2 Floating Plates
- 4 Capacitors in Series
- Reduction of Margin Stresses
- Some loss of effective area
- Same volts/mil Design Principles Apply

Internal Construction

7,500 VDC – 10,000 VDC

Non-Repairable Space Level Applications



- Series Parallel Design
- 3 Floating Plates
- 6 Capacitors in Series
- Reduction of Margin Stresses
- Same volts/mil Design Principles Apply

Testing and Screening Options of High Voltage Ceramic Capacitors

100% Group A Screening per MIL-PRF-49467C
Non- Repairable Space Level

- 5 Cycles Thermal Shock, -55°C – 125°C
- Dielectric Withstanding Voltage @ 1.5x ≤ 1250 VDC rated, 1.2x > 1250 VDC, 1.5x for Disc Capacitors
- Voltage Conditioning (Burn In) @ Rated Voltage and Temperature
- Insulation Resistance @ Rated Voltage and Temperature
- Insulation Resistance at 25°C
- Capacitance and Dissipation Factor at 25°C
- **100% Partial Discharge (Corona) Testing**
- Final Visual Inspection

100% SLAM/CSAM Ultrasound Testing Non-Repairable Hi-Rel Applications

- Ultrasound Waves are transmitted through the Capacitor
- Detection of flaws in the Capacitor such as voids, delaminations and cracks
- Expensive Process
- Sometimes used in conjunction with Partial Discharge Testing

Group B Sampling per MIL-PRF-49467C

Table VI. Periodic Group B Inspection

Inspection	Requirement Paragraph	Test Method Paragraph	Number of Sample Units to be Inspected		Number of Defectives Permitted 2/	
Subgroup 1 (every 6 months)						
Terminal strength	3.18	4.8.14	12	2/	1	1
Resistance to soldering heat	3.11	4.8.7				
Moisture resistance	3.19	4.8.15				
Subgroup 2 (every 6 months)						
Voltage-temperature limits 3/	3.14	4.8.10	6		1	
Low temperature storage	3.23	4.8.19				
Marking legibility (laser marking only)	3.25.1	4.8.1.1				
Subgroup 3 (every 6 months)						
Resistance to solvents	3.21	4.8.17	4/ 4		1	
Subgroup 4 (every 3 months)						
Life (at elevated ambient temperature) 2000 hours	3.22	4.8.18	10 minimum per style		1	
Partial Discharge	3.10	4.8.6				

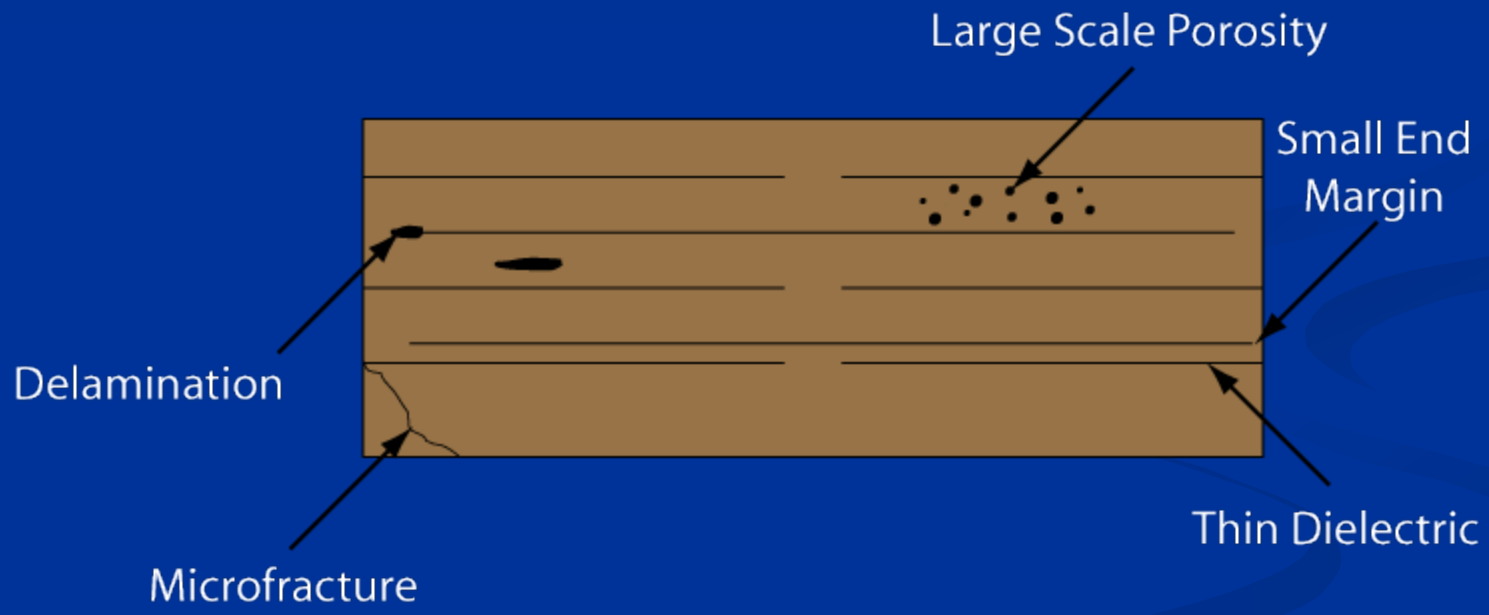
1/ A sample unit having one or more defects shall be charged as a single defective.

2/ Samples shall be representative of the highest capacitance value of each style manufactured during the sampling period.

3/ Samples shall be selected from a minimum of two lots per sampling period when more than one lot of dielectric is used.

4/ When more than one marking type is used (see 3.21), an additional four samples shall be added for each additional marking type.

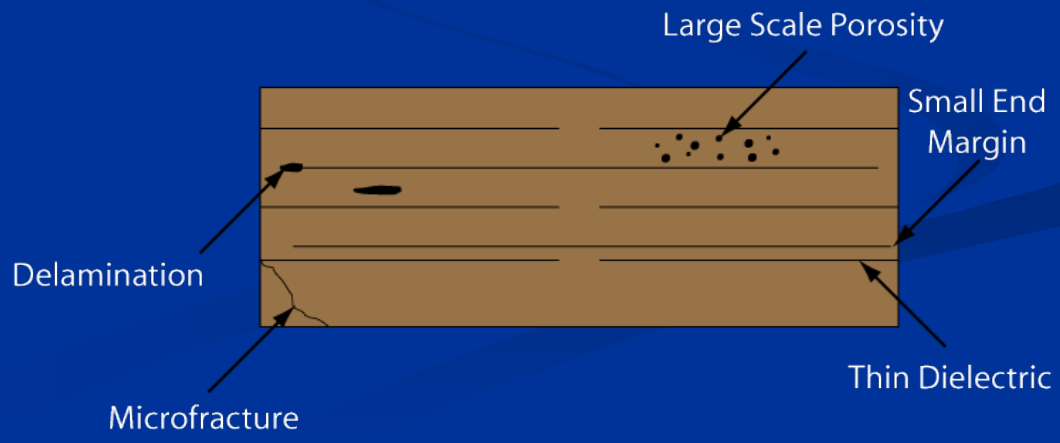
Potential Capacitor Flaws



Screening Options by Flaws

Group A, Mil prf-49467C (w/o Partial Discharge)

- Microfractures
- Large Delaminations
- Very Thin Dielectric
- Very Small End Margin



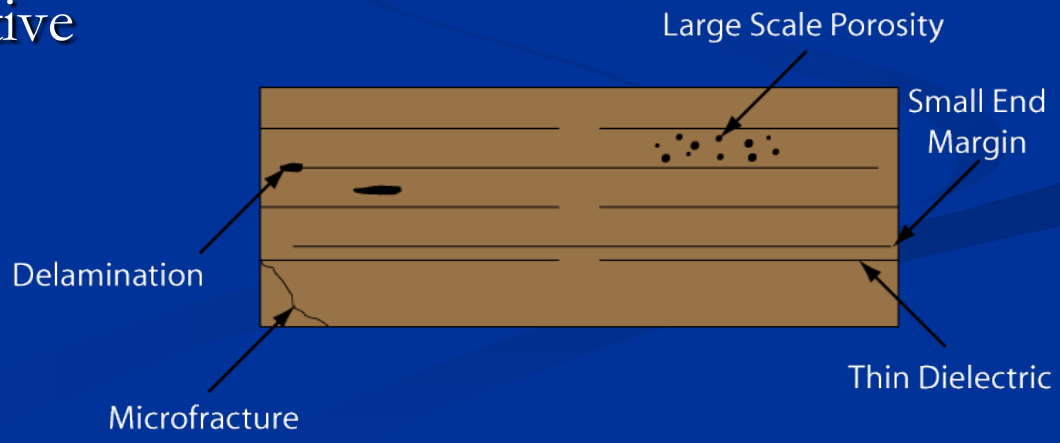
Screening Options by Flaws

Partial Discharge

- Microfractures
- Delaminations of Any Size in active area
- Thin Dielectric
- Large size Porosity in active area only
- Small End Margin

SLAM/C-SAM

- Large size Porosity or delaminations in all areas (cover plates)



Partial Discharge Overview

- Two primary breakdown mechanisms of ceramic capacitors are:
  - Electron Avalanche breakdown
  - Partial discharge Corona breakdown

Corona Breakdown

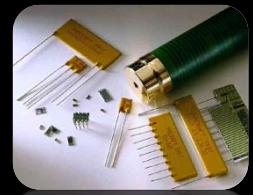
- Ionization of gas within a void or delamination caused by conduction of current across the flaw
- Governed by MIL-PRF-49467C, 0.42 x DC rating, tested @ VRMS, 60Hz, 25°C,
- 100 pico Coulombs maximum, continuous
- Applied voltages must be above Paschen's minimum of 320VRMS for Corona to occur
- Two types of Corona:
  - Townsend Type - Low intensity (10 pc), infrequent small spark, short duration
  - Streamer Type - Above CIV there is are continuous discharges, and may eventually lead to failure of the capacitor

References

- Bartnikas, R. and Mahon, E.J., Editors, "Engineering Dielectrics Volume I Corona Measurement and Interpretation", American Society for Testing and Materials, 1979, ATSM STP 669
- Boggs, S.A., "Partial Discharge: Overview and Signal Generation", IEEE # 0883-7554/90/0700-0033, 1990
- Day, J., Roach, M., and Maxwell, J., "Partial Discharge (Corona) Testing for High Voltage Ceramic Capacitors", Capacitor and Resistor Technology Symposium, March 1997, pp. 237-243
- MIL-PRF-49467C, Military Specifications, Capacitors, Fixed, Ceramic, Multilayer, High Voltage (General Purpose) Established Reliability, General Specification For
- EIA-469-C, Standard Test Method for Destructive Physical Analysis (DPA) of Ceramic Monolithic Capacitors

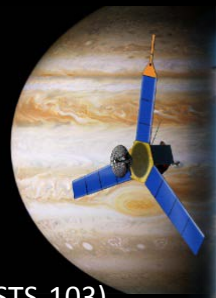
Introducing Allen Drumheller to Discuss the Design and Proper Application of Specialty High Voltage Resistors

OHMCRAFT Space Applications



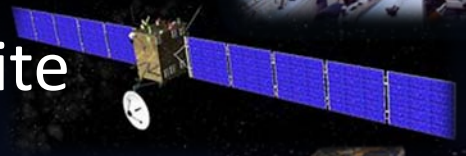
- MSL– CheMin, SAM

- Juno – JADE, JEDI

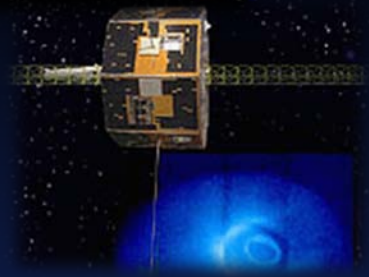


- Hubble Space Telescope (December 1999 repair STS-103)

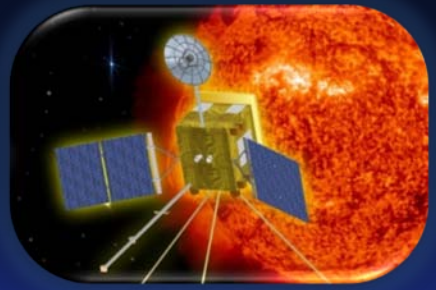
- Rosetta, the Comet-Chasing Satellite



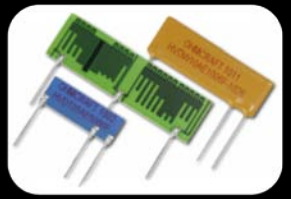
- IMAGE Satellite (Imager for Magnetopause-to-Aurora Global Exploration)

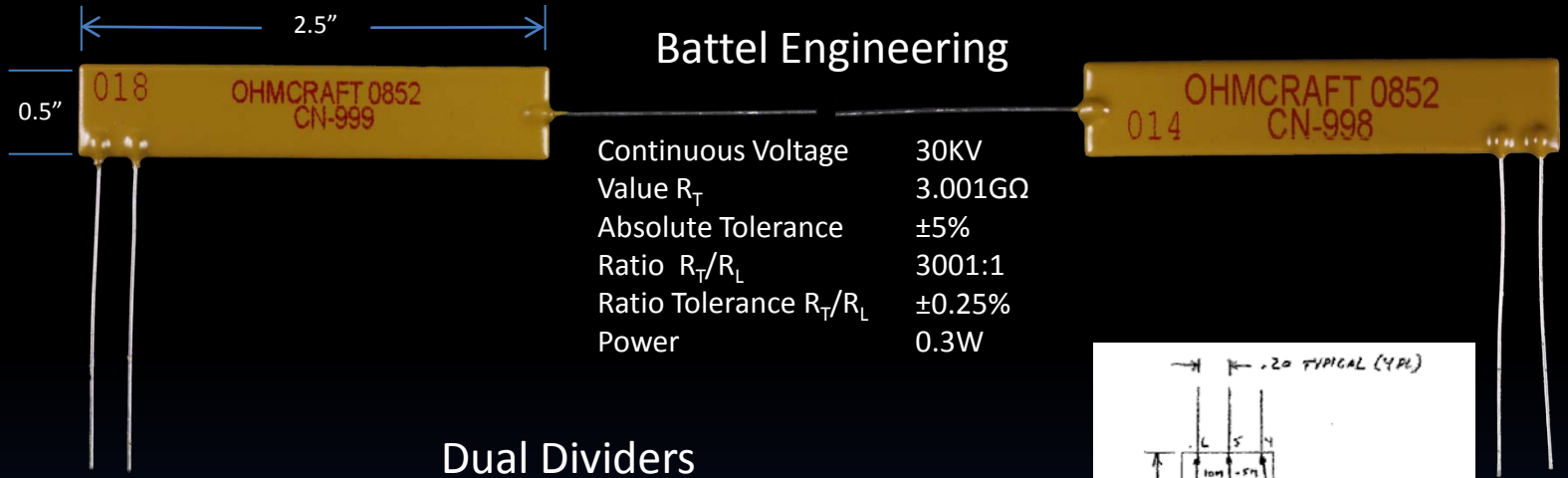


- Solar Orbiter - SWA



High Voltage Leaded Resistors

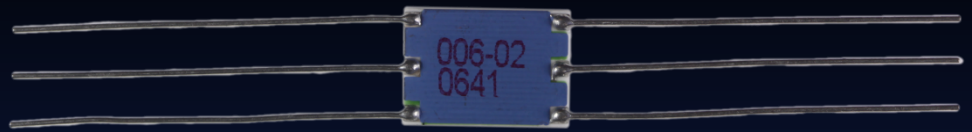




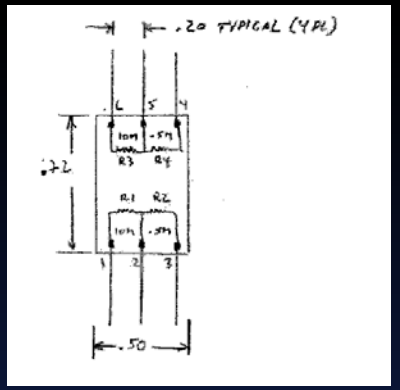
Battel Engineering

Continuous Voltage	30KV
Value R_T	3.001GΩ
Absolute Tolerance	±5%
Ratio R_T/R_L	3001:1
Ratio Tolerance R_T/R_L	±0.25%
Power	0.3W

Dual Dividers

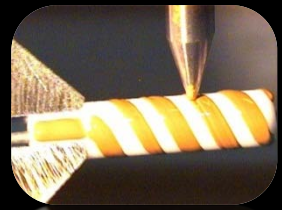


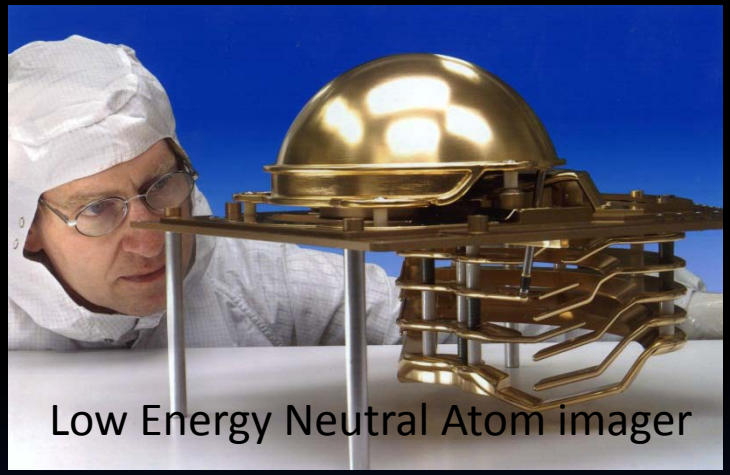
Continuous Voltage	2000V
Value R_T	10.5MΩ
Absolute Tolerance	±1%
Ratio R_T/R_L	21:1
Ratio Tolerance R_T/R_L	±1%
Power	0.3W
Size	0.5 x 0.72”

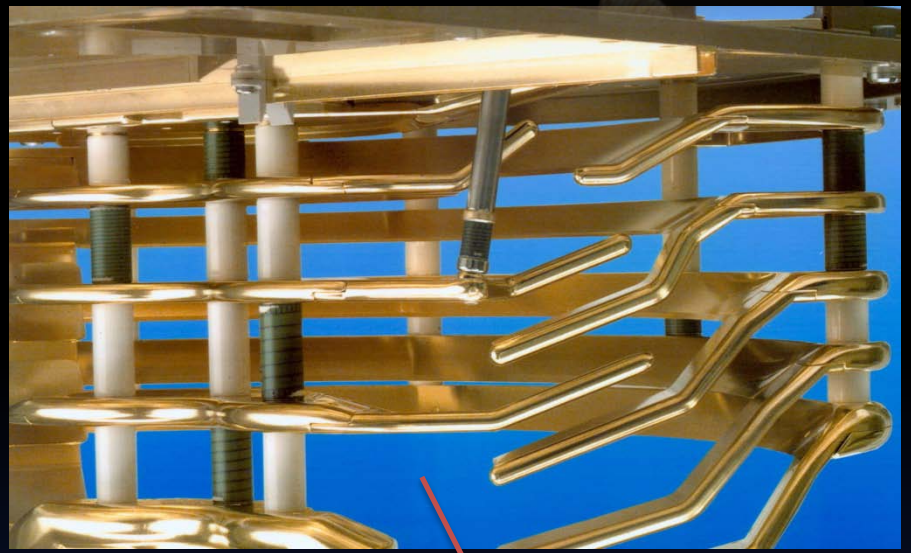


S. J. Battel
Drawing From
Procurement Specification

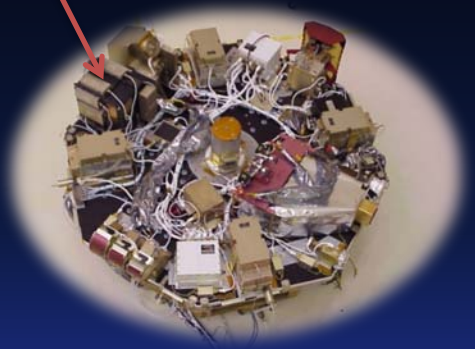
Non-Traditional Resistors



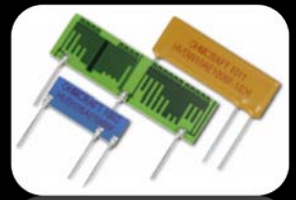


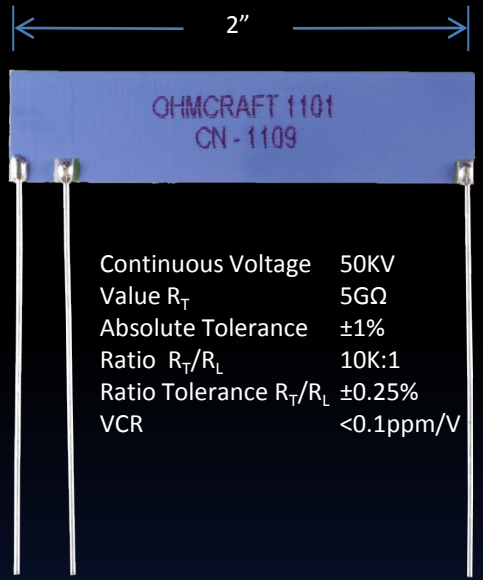


Lockheed Martin Missiles & Space Co.
8 Unique parts ranging from 539MΩ to 11.138GΩ ±1%
The resistor are part of the structure of the LENA instrument
LENA was 1 of 7 instruments on the IMAGE Spacecraft
Ohmcraft had parts in at least 3 instruments

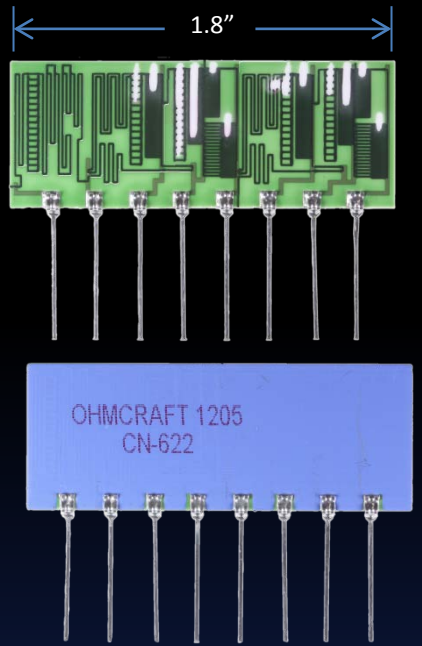


High Voltage Leaded Resistors

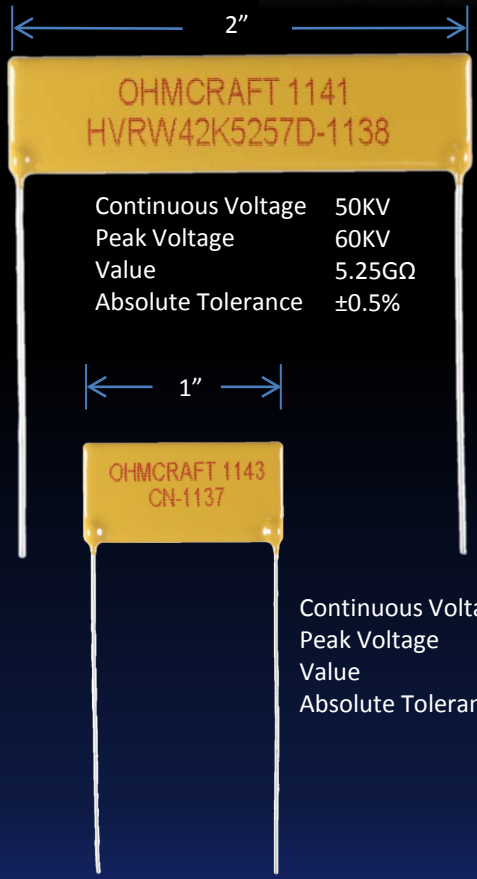




Continuous Voltage	50KV
Value R_T	5GΩ
Absolute Tolerance	±1%
Ratio R_T/R_L	10K:1
Ratio Tolerance R_T/R_L	±0.25%
VCR	<0.1ppm/V



1GΩ to 1KΩ Decade Divider
Ratio Tolerance 0.25%
TCR Tracking 25ppm/°C
Voltage 1000V



Continuous Voltage	50KV
Peak Voltage	60KV
Value	5.25GΩ
Absolute Tolerance	±0.5%

Continuous Voltage	25KV
Peak Voltage	30KV
Value	2.625GΩ
Absolute Tolerance	±0.5%

Surface Mount Resistors

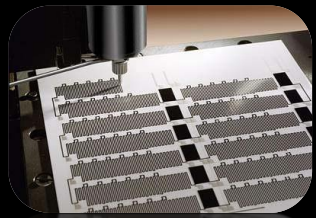
Continuous Voltage	50KV in oil
Value R_T	20GΩ
Absolute Tolerance	±1%
VCR	<0.5ppm/V

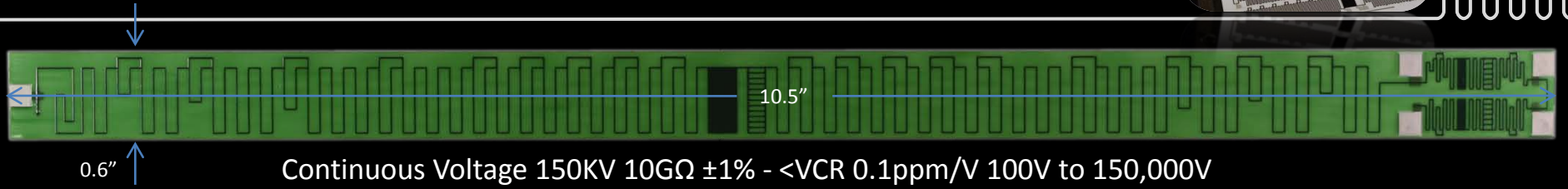
HVC2010M1203FB
120KΩ
2500V 20ms Pulse
3 Joule

HVC3508H3306FB
330MΩ
10KV

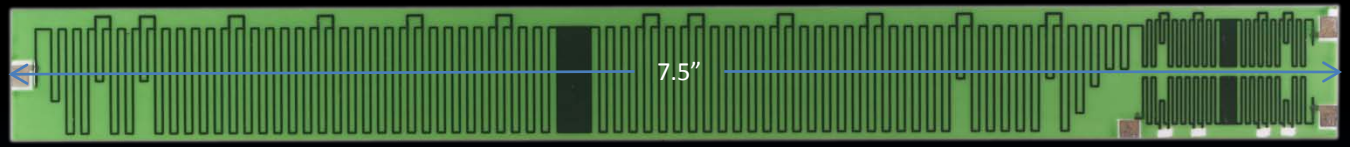
HVC2510K8756FT
875MΩ
8.5KV
VCR <3ppm/V

150KV Resistor

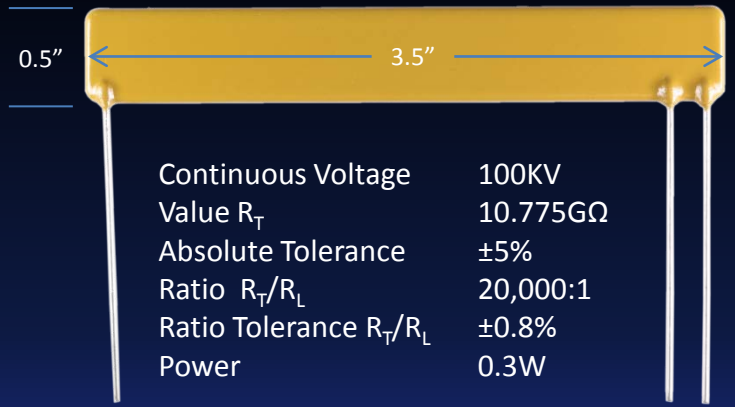




Continuous Voltage 150KV 10GΩ ±1% - <VCR 0.1ppm/V 100V to 150,000V

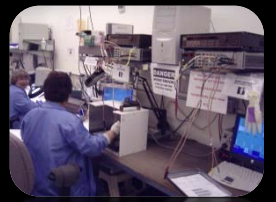


Continuous Voltage 120KV 10GΩ ±1% - VCR <0.1ppm/V 100V to 120,000V



Continuous Voltage	100KV
Value R_T	10.775GΩ
Absolute Tolerance	±5%
Ratio R_T/R_L	20,000:1
Ratio Tolerance R_T/R_L	±0.8%
Power	0.3W

Lot Acceptance Testing



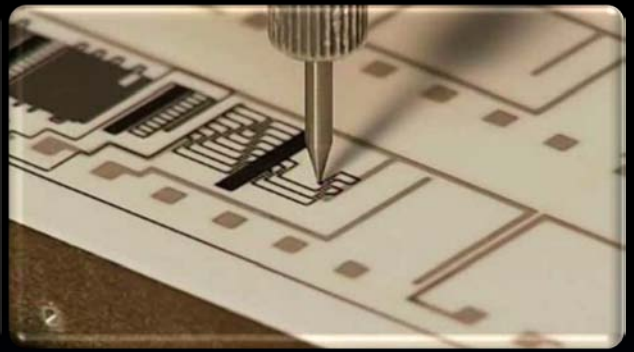
Typical LAT Data

Thermal shock	0.02%
Low temperature operation	0.01%
Short time overload	0.05%
High temperature exposure	0.01%
Resistance to soldering heat	0.05%
Moisture resistance	0.01%
Life Qualification	0.01% to 0.15%*

* High wattage parts can shift more than others

Micropen at Work

Product	Gas heater
Substrate	Quartz
Flowable Material	Pt ink
Application	Gas chromatography
Line Width	875µm



Product	Endotracheal tube
Substrate	DEHP-free PVC
Flowable Material	Polymeric Ag ink
Application	Bio-impedance
Line Width	625µm

Product	Conical/Square balloon
Substrate	Urethane
Flowable Material	Polymeric Ag ink
Application	Ablation
Line Width	250µm

Product	Electrocauterization Probe
Substrate	7 FR, 96% Alumina ceramic, bullet shaped
Flowable Material	Gold-filled cermet conductive ink
Pattern	Bipolar helix, 250 micron line width

Product	Immersion heater
Substrate	Stainless steel
Flowable Material	Dielectric, Ag conductor and resistor inks
Application	Cauterization
Pattern	6 layer pattern with helical heater, 375µm line width, 1125µm pattern width

Introducing Dave McCormick to Discuss Considerations in the Selection of High Voltage Cables and Connectors

Space Level Interconnect Components

Dave McCormick

Director of Engineering

Teledyne Reynolds, Inc

5005 McConnell Ave.

Los Angeles, CA 90066

- ***High Voltage Interconnections***
- ***High Voltage Wire***
- ***Hybrid Cable Assemblies***
- ***Ceramic to metal Brazed Interconnects***
- ***High Voltage Mica Capacitors***

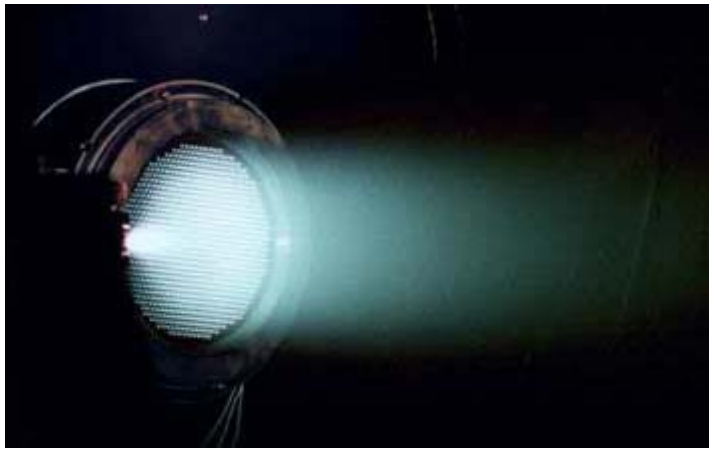
Space Level Products

Agenda

- Applications
- Definition of space level component
- Connector features
- Voltage rating
- Environment
- Configuration
- Processes
- Testing
- Data
- Types of Interconnects
- Application Notes (Technical Bulletins)
- Capacitors

Typical Applications

- Propulsion
  - Electrostatic Ion Thrusters
  - Electromagnet Ion Thrusters
  - Electro thermal (Arcjet) Thrusters
  - Electrodynamic Tethers
  - Pulse Detonation Engines
  - Spark Igniters
- Mass Spectrometers
- Radar
- Detectors
  - Photomultiplier tubes (PMT)
  - Microchannel Plates (MCP)
  - Avalanche Photo Diodes (APD)

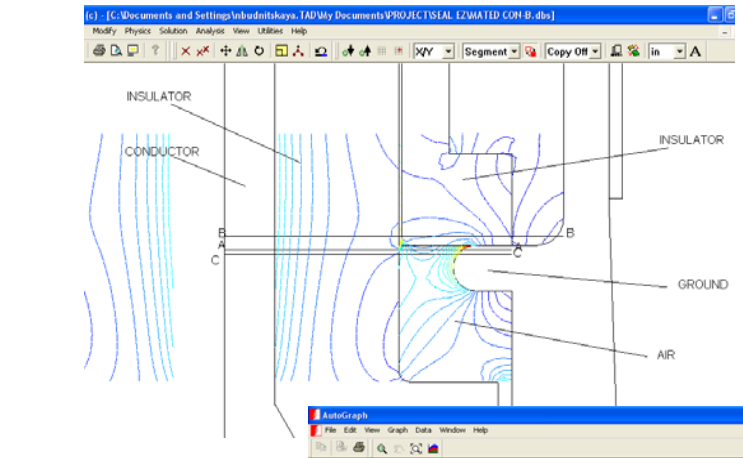


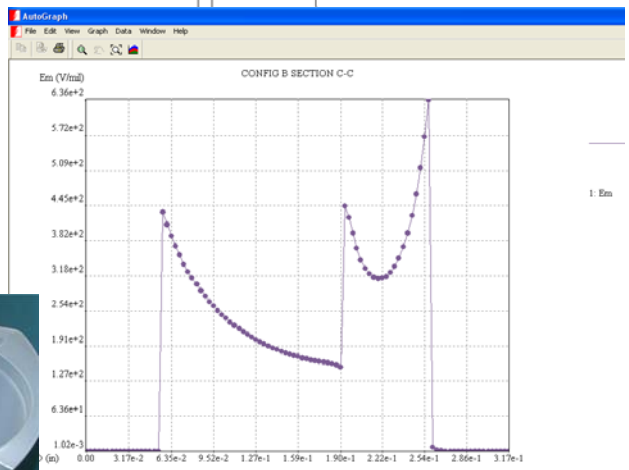
What constitutes a ‘space level’ HV connector?

- Reliability
  - Lot traceability
  - Screening
  - Supporting data
- Vented / non vented
- Low outgassing (TML <1%; CVCM <0.1%)
- High purity insulation
- Hermetic – some cases
- Red plague resistant (silver plate thickness) – *sometimes*
- Non magnetic metals
- No pure tin

How is this achieved?

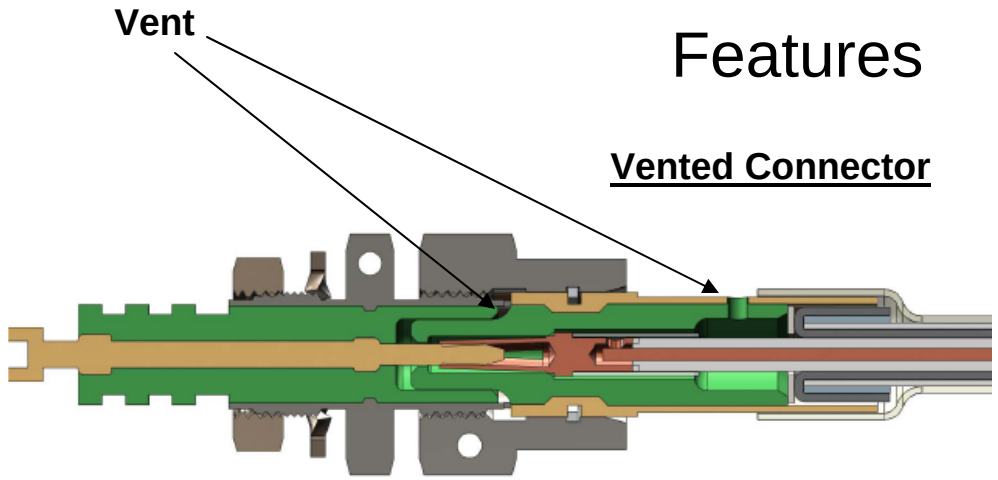
- Knowing the induced voltage stress & margin
  - Electrostatic analysis & test data
- Knowing the characteristics of the material & process used
  - Laboratory / verification methods
  - Database of materials & processes
  - Outgassing
- Solid modeling design & analysis
- High voltage testing
  - Dielectric withstanding voltage (DWV)
  - Insulation Resistance
  - Corona / Partial Discharge
- Qualification tests

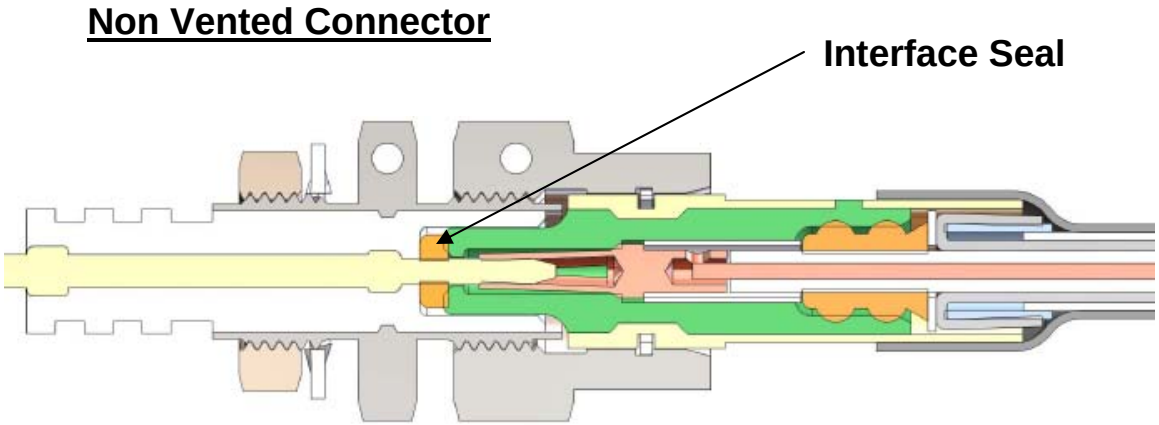




Connector Features

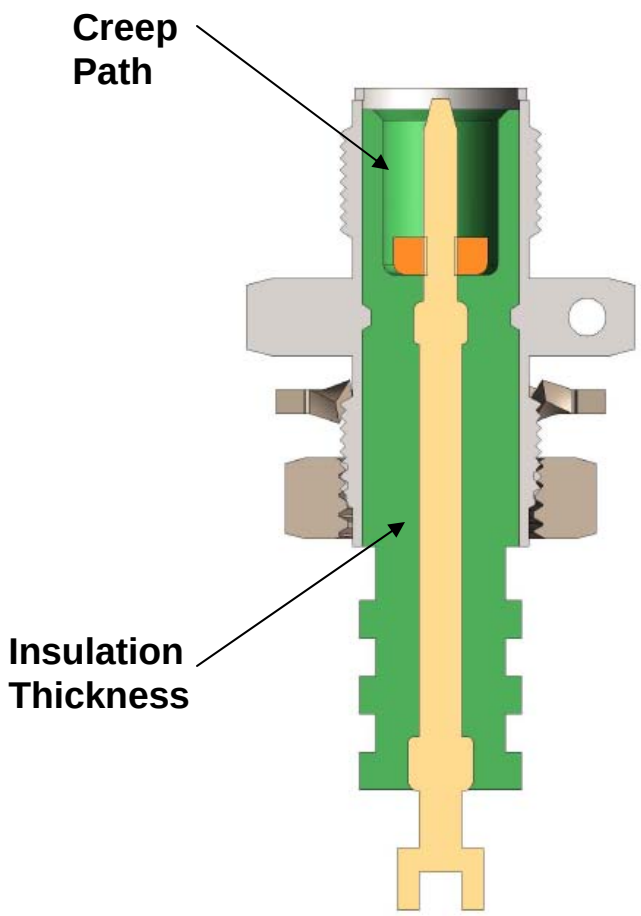
- Configuration
  - Single pin
  - Multi-pin
  - Shields
- Vented vs. non vented
  - Paschen curve
- Voltage rating
  - Margin of safety
- Environments
  - Natural
  - Induced
- Hermetic





Connector
Voltage Rating

- Type of insulation
  - Temperature capability
  - Dielectric Strength
    - Most polymers are measured at 60Hz AC
    - AC to DC: 1:2 to 1:4
  - Volume Resistivity
    - Low volume resistivity / higher leakage current
  - TML & CVCM
    - Some are on NASA website others are tested
- Thickness of insulation surrounding conductors
- Edge effects
  - Sharp corners induce high voltage stresses
  - ~ d/D
- Air voids – source of ionization
  - Common
  - Induced by processes
- Creep path
  - Interface
  - Substrates
- Interface compression (‘non’ vented connectors)



Environmental

- Pressure
  - Sea level / vacuum / Paschen curve
- Temperature
  - Operating
  - Storage / Non Operating
  - Dwell times
- Humidity / Moisture
- Hermeticity: Specify differential pressure condition and the acceptable leak rate.
- Thermal Cycling: Specify extremes, dwell time, rate of change and number of cycles.
- Dielectric Fluids and Gases:
  - Fluids should be specified with the degree of exposure.
  - Exposure can range from vapors, to splash, to total immersion.
  - Specify whether or not the connector is required to seal the dielectric from escaping.
- Radiation: Specify the type, level and dose rate

Connector
Mechanical

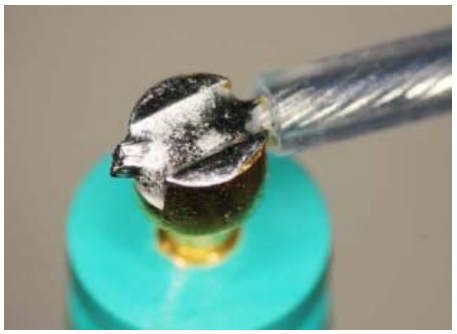
- Threaded / Bayonet
  - Mating cycles
- Material - metallic
  - Non magnetic
- Finishes
  - Plating (if not stainless)
  - Red plague
- Durability
  - Consider plating

Gold Plated Brass 600

Stainless 600 Series

Connector Processes

- Soldering
  - J STD 001E/S & Company standards
  - Special attention to sharp corners /excessive flux
- Material analysis
  - Surface adhesion / bonding
    - Voltage withstanding proportional to adhesion strength
- Rubber & plastic molding
  - Voids
- Ceramic to metal brazing
- Altitude – vacuum testing
- Corona testing
- Encapsulation
- Wire – reel to reel cable screening
  - Detecting voids / contamination



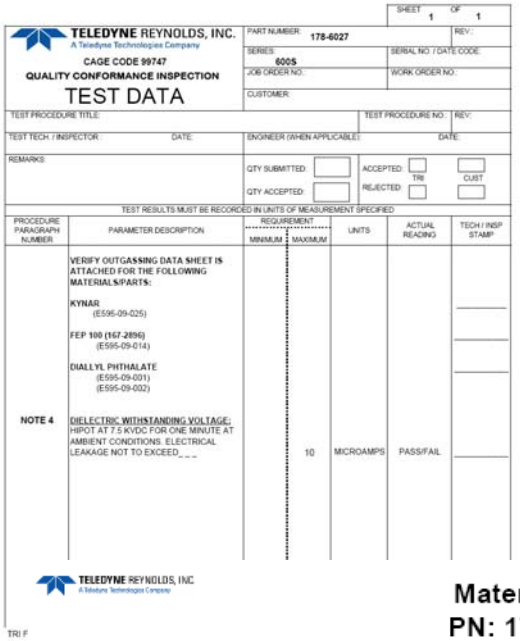
Connector
Testing & Validation

- Dielectric Withstanding Voltage (See Table)
  - Leakage current
- Insulation Resistance
  - 500VDC; varies depending on insulation thickness
  - Before and after DWV
- Circuit Resistance
  - Not just continuity; to assure all terminations are good
- Real time X ray
- Space simulation
- Screening
  - Thermal cycling
  - Partial discharge

DC Rating	Test Voltage Percent of Rating
0 – 12 kVDC	150%
12.1 – 20 kVDC	140%
20.1 – 30 kVDC	130%
≥ 30.1 kVDC	120%

Connector Data

- Test Reports
- Material & Process Data List
- X Ray
- Lot control



TELEDYNE REYNOLDS, INC.
A Teledyne Technologies Company

CAGE CODE 99747
QUALITY CONFORMANCE INSPECTION
TEST DATA

PART NUMBER: 178-6027 REV:
SERIES: 600S SERIAL NO / DATE CODE:
JOB ORDER NO.: WORK ORDER NO.:
CUSTOMER:
TEST PROCEDURE TITLE: TEST PROCEDURE NO.: REV:
TEST TECH / INSPECTOR: DATE: ENGINEER (WHEN APPLICABLE): DATE:
REMARKS: QTY SUBMITTED: QTY ACCEPTED: ACCEPTED: TRI CUST REJECTED:

TEST RESULTS MUST BE RECORDED IN UNITS OF MEASUREMENT SPECIFIED

PROCEDURE PARAGRAPH NUMBER	PARAMETER DESCRIPTION	REQUIREMENT MINIMUM	REQUIREMENT MAXIMUM	UNITS	ACTUAL READING	TECH / INSP STAMP
	VERIFY OUTGASSING DATA SHEET IS ATTACHED FOR THE FOLLOWING MATERIALS/PARTS:					
	KYNAR (E595-09-025)					
	FEP 100 (167-2896) (E595-09-014)					
	DIALLYL PHTHALATE (E595-09-001) (E595-09-002)					
NOTE 4	DIELECTRIC WITHSTANDING VOLTAGE: HIPOT AT 7.5 KVDC FOR ONE MINUTE AT AMBIENT CONDITIONS. ELECTRICAL LEAKAGE NOT TO EXCEED_ _ _		10	MICROAMPS	PASS/FAIL	

TELEDYNE REYNOLDS, INC
A Teledyne Technologies Company

TRI F

Test Data Sheet

X Ray Screen

Material List
PN: 178-5996

TRI P/N	Description	Material	Finish	Comments
178-5996	SINGLE ENDED PLUG CABLE ASSEMBLY, SPACE RATED, 600S SERIES			
R-500-4	INK, EPOXY, BLACK	MARKEM 7906, BLACK		
SN60A	SOLDER	SN60PB40 SOLDER		
178-2881-1	SHRINK TUBING (ID SLEEVE)	CLEAR KYNAR IAW AMS-DTL-23053/8		MEETS ASTM E595
167-2896	HIGH VOLTAGE COAXIAL CABLE TYPE "L" Ø.050 CORE FEP	CENTER : 19 STRANDS OF 38 AWG COPPER WIRE PER MIL-C-17. INNER INSULATION: FEP 100, NATURAL BRAID: COPPER BRAID PER MIL-C-17 JACKET: FEP 100, WHITE	CENTER: SILVER PLATED IAW ASTM B298 BRAID: SILVER PLATED IAW ASTM B298	MEETS ASTM E595
178-2881	SHRINK TUBING	CLEAR KYNAR IAW AMS-DTL-23053/8		MEETS ASTM E595
167-3541-1	U-SLEEVE	COPPER IAW ASTM B152, COLD ROLLED ANNEALED.	SULFAMATE NICKEL IAW SAE AMS-QQ-N-290 CLASS 2, .0001-.0003 THK	
167-4112	WASHER	301 STAINLESS STEEL PER QQ-S-766	PASSIVATED PER QQ-P-35, TYPE VI OR VII	
178-4924	SPACER INSULATOR	ULTEM 1000 (ASTM D 5205)		MEETS ASTM E595
167-4602	CONTACT, 600 SERIES	COPPER ALLOY IAW ASTM B196, UNS C17200 OR C17300, TEMPER TD04.	COPPER UNDERPLATE IAW SAE AMS 2418, .0001-.0002 THICK FOLLOWED BY GOLD PLATE IAW ASTM B488, TYPE 3, CODE C, .000050-.00010 THICK	
167-4834	RETAINING RING	BERYLLIUM COPPER IAW ASTM B197, UNS C17200 BAR-ROUND, TEMPER TD04 OR IAW ASTM B194, TEMPER TD02.		
167-7094	COUPLING NUT	303 STAINLESS STEEL IAW ASTM-A-582, CONDITION A, OR 303se IAW ASTM-A-581	PASSIVATED PER QQ-P-35	
167-4605	MOLDED ASSY	MOLD MAT'L: DIALLYL PHTHALATE PER ASTM D 5948, TYPE SDG		MEETS ASTM E595
167-4600	BODY, 600 SERIES	BRASS 1/2 HARD PER QQ-B-626 COMP. 22 (ALLOY 360)	GOLD PLATE IAW SAE AMS 2422, .000050 IN MIN THICK, OVER COPPER SUBPLATE IAW SAE AMS 2418, .000100 IN MIN THICK.	

Material & Process Data List

Space Level Interconnects

Model	Cond	Style	Shell Type	Coupling	Insulation Type	Voltage DC	Shield
600	1	Plug	Brass/Au	Threaded	Plastic	5kV	Yes
600	1	Plug	CRES	Threaded	Plastic	5kV	Yes
600	1	Receptacle	Brass/Au	Threaded	Plastic	5kV	Yes
600	1	Receptacle	CRES	Threaded	Plastic	5kV	Yes
600	1	Receptacle	CRES	Threaded	Ceramic	5kV	Yes
600	1	Adapters	Brass/Au	Threaded	Plastic	5kV	Yes
311	1	Plug	Brass/Au	Bayonet	Plastic	15kV	Yes
311	1	Receptacle	Brass/Au	Bayonet	Plastic	15kV	Yes
Pee Wee	1	Plug	N/A	Push/Pull	Plastic	12kV	No
Pee Wee	1	Receptacle	N/A	Push/Pull	Plastic	12kV	No
Pee Wee	1	Receptacle	N/A	Push/Pull	Ceramic	12kV	No
Cable	NA	NA	N/A	NA	FEP/PFA	18kV	Y/N
1807	7	Plug	Electroless Nickel	Threaded or Bayonet	Silicone	15kV	Y/N
1807	7	Receptacle			Plastic	15kV	Y/N

Cable – Wire

Materials

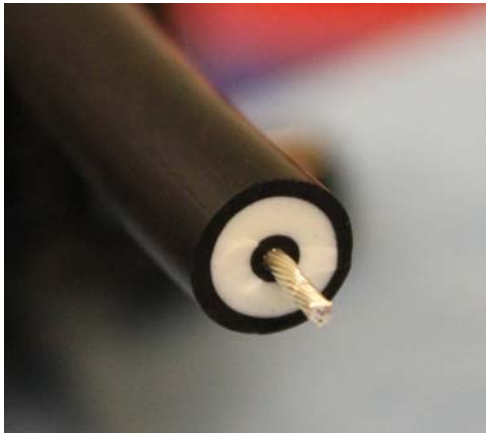
Property	FEP	PFA	Silicone
Specific Gravity Nom	2.15	2.14	1.15-1.38
Dielectric Strength (V/mil)	500	500	575 - 700
Dielectric Constant- Nom	2.1	2.0	3.6
Abrasion Resistance	Excellent	Excellent	Fair
Flame Retardant Properties	Excellent	Excellent	Excellent
Flexibility	Very good / size	Very good / size	Excellent
Temperature*	-70C to +200C	-70C to +200C	-65C to +200C
Resistance to Chemicals	Excellent	Excellent	Fair to good

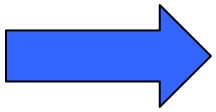
Insulation resistance vs. high temperature

Cable - Wire

Insulation Type	Surface	Precoat	Environment
FEP/PFA	None	None	Non potted
FEP/PFA	Etched	None	Epoxy/polyurethanes / some silicones
FEP/PFA	Etched	Silicone	Silicone
Silicone	None	None	Non potted or silicone
Dual Layer Silicone	None	None	Non potted or silicone

FEP/PFA Cable





Semicon Layered Cable

Application Notes

Technical Bulletins

TB10-024	Allowable Wire Bend Radius
TB10-025	When to use plain FEP, etched FEP and silicone coated FEP
TB10-026	Soldering (recommended irons or wattage) 600 Series
TB10-027	Soldering (recommended irons or wattage) Pee Wee Series
TB10-028	Connector interface maintenance 600 Series
TB10-029	Connector interface maintenance Pee Wee Series
TB10-030	Mating Pee Wee Connectors
TB10-031	Replacing 600 interface seals
TB10-032	Mating 600 Series Connectors
TB10-033	Post baking
TB10-034	Mounting guidelines for Pee Wee receptacle
TB10-035	Mounting / retaining of Pee Wee plug cable assemblies
TB10-036	Surface quality of high voltage insulators
TB10-037	Packaging and storing of space level connectors
TB10-038	Space Level Non Metallic Materials - Properties / Plastic & Rubber
TB10-039	Ink Properties/Ink/Shrink Sleeves

HV Mica Capacitors

- Mica paper 0.018 – 0.05 mm (0.007 -.002 inch?)
- Wound with capacitor grade aluminum foil and epoxy impregnated
- 50pF to 5micro F
- 2kVDC – 50kVDC
- -55C to +125C
- White paper
  - Reliability & Design Considerations HV Mica Capacitors
  - Life Test / Reliability Results HV Mica Capacitors

High Voltage Mica Capacitors

Rated DC Voltage (kV)	DC Test Voltage (kV) % of Rated
0 to 8.0	200
8.1 to 10.0	175
10.1 to 12.9	150
12.1 to 20.0	140
20.1 to 30.0	130
30.1 to 45.0	120
45.1 and up	110

Note: some testing in the higher voltage regions will warrant immersion of the capacitor under test into a dielectric fluid or gas to prevent flashover from one termination point to another. This is dependent upon the form factor of the device under test and room ambient conditions such as relative humidity.

Contacts

- Technical Service:
  - www.teledynereynolds.com
    - Technical Information Request / Technical Support Request
    - Home page; HV Wire & Cable; Legacy Group; Advanced Group
- Connector, wire & cable
  - Cesar Aldana
    - caldana@teledynereynolds.com
    - 310-823-5491 X359
  - Dave McCormick
    - dmccormick@teledyne.com
    - 310-823-5491 X232
- Capacitors
  - Jim McCoskey
    - jmccoskey@teledyne.com
    - 805-928-5866 X 11

Introducing Eric Hertzberg Discussing Physics-Based Design and Engineering Principles for High Voltage Insulation Systems

Life may not be fair but at least physics provides a level playing field!

High Voltage Design for Space Applications

Eric Hertzberg and Tom Sanders

Lockheed Martin Advanced Technology Center, Palo Alto CA

2 Apr, 2012

Table of Contents

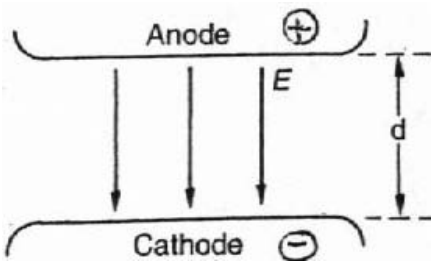
Fundamental Concepts

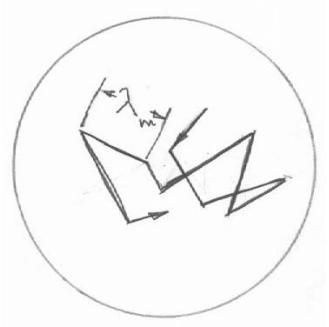
Introductory Comments

- A discussion of the behavior of Rarified Gasses in the Presence of Conductors, Insulators and Electric fields
  - DC conditions
  - AC: same physics, plus time domain effects
    - Usually aggravates DC effects
  - Field of interest is still evolving
  - Many variables
- Objective: design for zero discharge
  - Trouble-free design

Concepts of Gas Discharge, p1

- Imagine a Breakdown Test Apparatus
  - Parallel plate capacitor
  - Air in gap
    - "Gas dielectric"
    - No solid dielectric

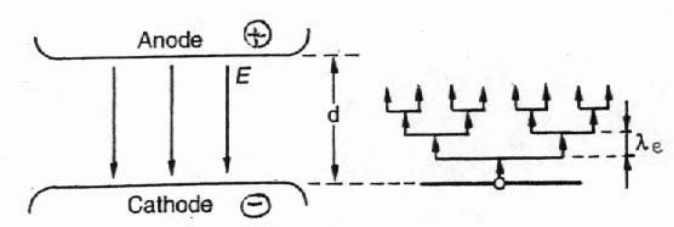




- Gas behavior:
  - Molecules move in random collisional motion (Brownian)
    - Average distance between collisions = Mean Free Path, λ_m
  - Molecules can be ionized if
    - We impart energy, ϵ, > molecular ionizing energy, ϵ_{mi}
      - ϵ_{mi} for N2 ≈ 15 eV
      - An electron is stripped off the molecule
- Apply high voltage (HV) across the capacitor
  - Imposes an electric field between plates
    - Distribution of potential energy around conductive elements

Concepts of Gas Discharge, p2

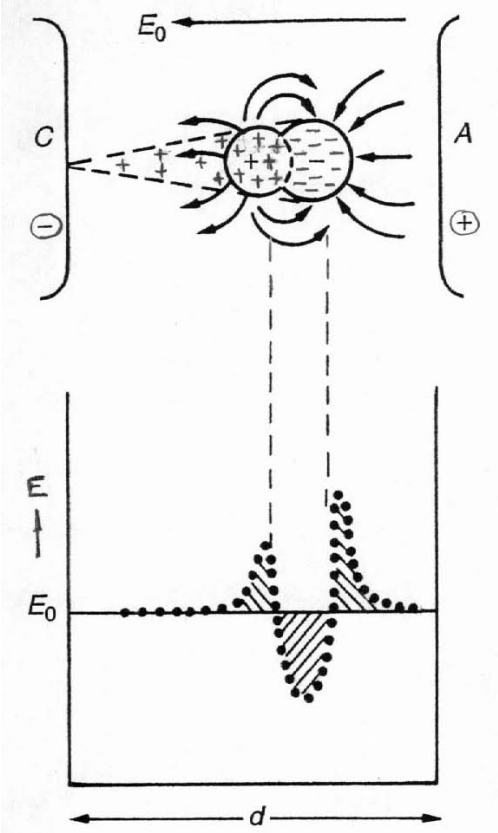
- Add a free electron into the capacitor gap
  - Electron has some λ_e in the gas environment
  - Attraction aligns λ_e with local electric field line toward + contact
    - Electron thermal energy << molecular ionization energy
  - Electron gains mean energy ϵ_{ef} from the electric field between collisions
    - ϵ_{ef} is proportional to λ_e
    - Convenient units: electron-volts
      - Apply to both + and – charges
  - If ϵ_{ef} > molecular ionization energy, ϵ_{mi}
    - Good probability of electron ionization of a gas molecule at the next collision
  - Once that happens we have 2 free electrons
  - Process repeats, causing an avalanche



Schematic representation from
Kuffel, Zaengl and Kuffel

Concepts of Gas Discharge, p3

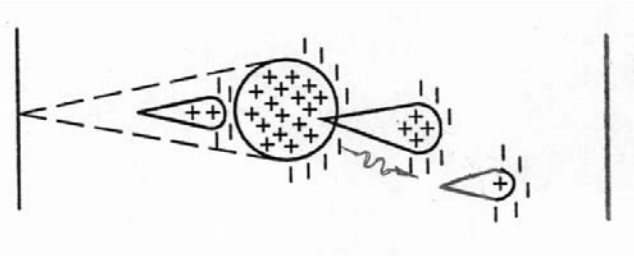
- Avalanche: onset of discharge:
  - Electrons are highly mobile (low mass)
  - Ions are ponderous (relatively high mass)
  - Electron cloud expands
    - From space charge repulsion
  - Dramatic field distortions
  - Dynamic conditions
  - Complex and random
- Dominant breakdown initiation mechanism
  - Kinetic electron ionization of ambient molecules
    - Townsend discharge



Plot from Kuffel, Zaengl and Kueffel

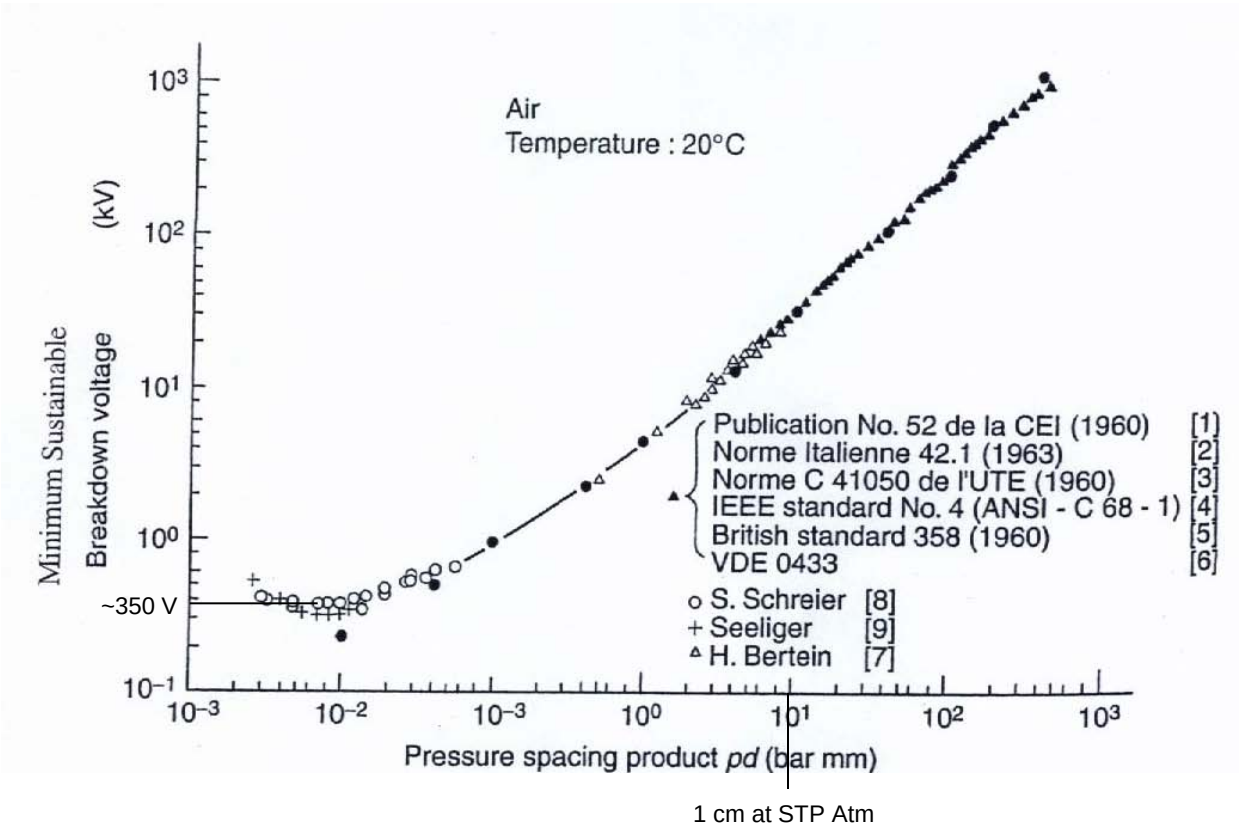
Concepts of Gas Discharge, p4

- When an electron is captured by an ion, or
- An excited molecule relaxes
  - Photon is emitted
  - Photons => photo ionization of gas => electrons =>more avalanches



The Paschen Curve, p1

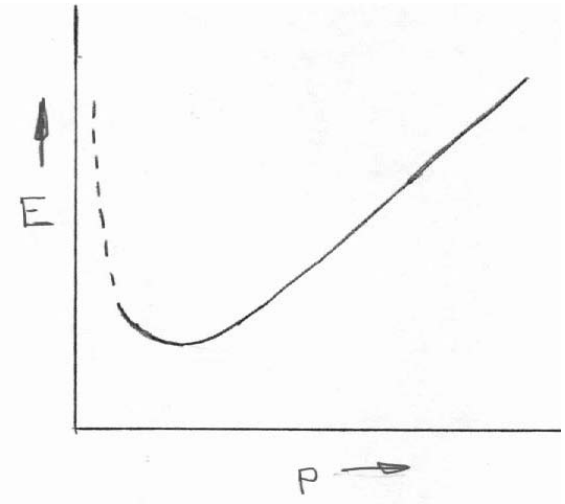
- Louis Carl Heinrich Friedrich Paschen
  - 1889, thesis work
- Why these units?
- Where is electric field?



Paschen curve for air at 20° C; solid dots are calculated using Townsend gas theory. Plot from Kuffel, Zaengl & Kuffel

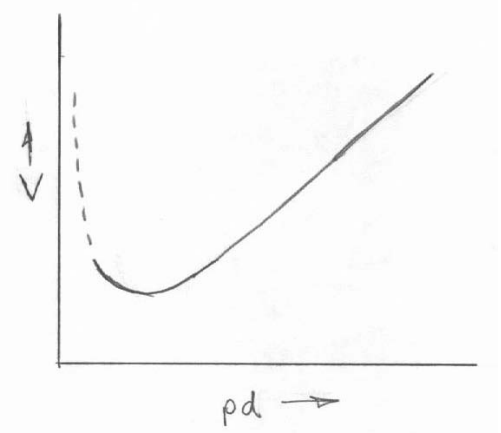
Paschen Curve, p2

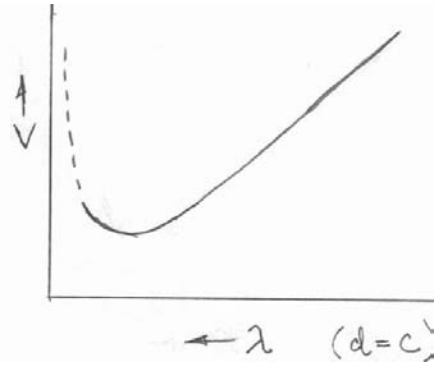
- Paschen used a uniform field
  - So E= V/d
- Curve can be presented as E vs p
- “Minimum Sustainable Breakdown Voltage”, “V”
  - Challenging to define
  - Depends on measurement sensitivity



Paschen Curve, p3

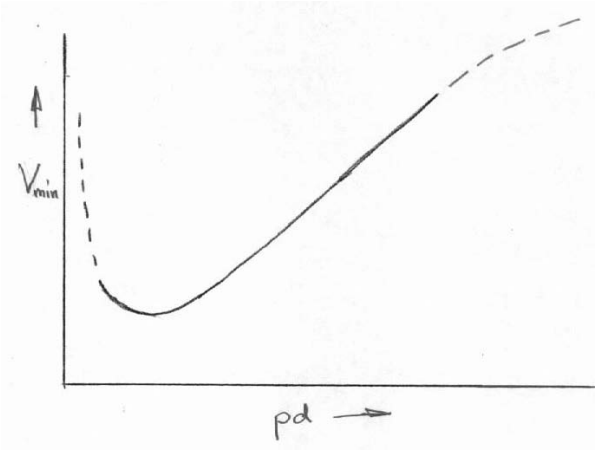
- Gross oversimplification
  - 45° slope region
    - Consider d and p separately
      - With second parameter held constant
    - d: Ionizing field, E_i = “V”/D = C
      - Gas property
      - “V” proportional to d
    - p: Ionizing ϵ_{mi} = K
      - Gas property
      - p proportional to 1/λ,
      - “V” proportional to 1/λ,
      - “V” proportional to p
    - Similarly for the product
      - Handy equation: λ_m [cm]*p[T] = 5 x 10^{-3}





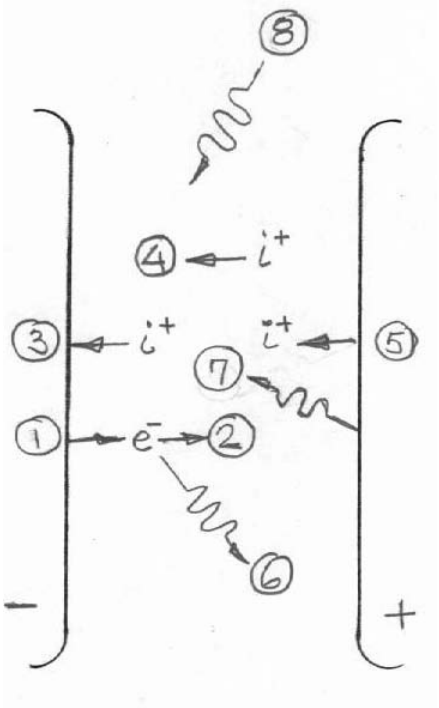
The Paschen Curve, p4

- Ends of curve
  - Minimum at low pd:
    - When $d \approx \lambda_{ei}$:
      - Most electrons strike anode
      - Few ionize gas molecules
      - Other mechanisms operate
        - » With lower ionization probability
    - "V" must rise
  - Right end
    - Other mechanisms take over
    - Curve rolls off to right



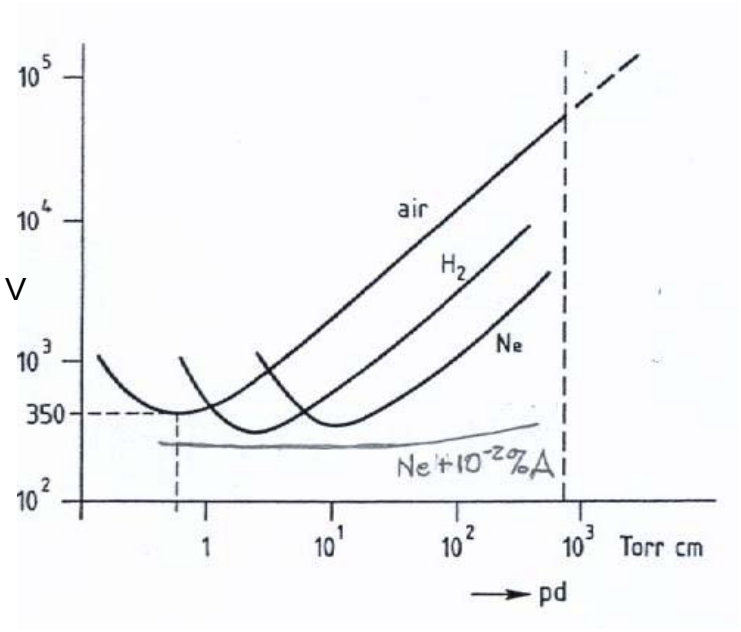
Paschen Curve, p5

- In reality, many ionizations sources:
  - By accelerated electrons
    1. Emitted from cathode (dominant initiation source)
    2. From avalanches (dominant continuation mechanism)
  - By discharge ions
    3. Striking cathode, releasing electrons
    4. Further ionizing gas molecules
    5. Emitted from anode (fields > ~20 kV/mm)
  - By photons
    6. Released by recombination processes
    7. From anode and cathode
    8. From environment (sun, other discharge, etc.)
  - Other sources of initiating electrons
    - Penetrating charged particles/cosmic rays
    - Intrinsic radio-activity of construction materials



The Paschen Curve, p6

- Everything changes if any of following vary:
  - Parallel field geometry
    - Typical electronics geometries => lower “V”
  - Temperature
  - Gas mixture
    - Particularly humidity in air
  - Contact material



Plot from Kreuger

- Paschen is known because he controlled all the variables that would have destroyed his systematic results.

The Paschen Curve, p7

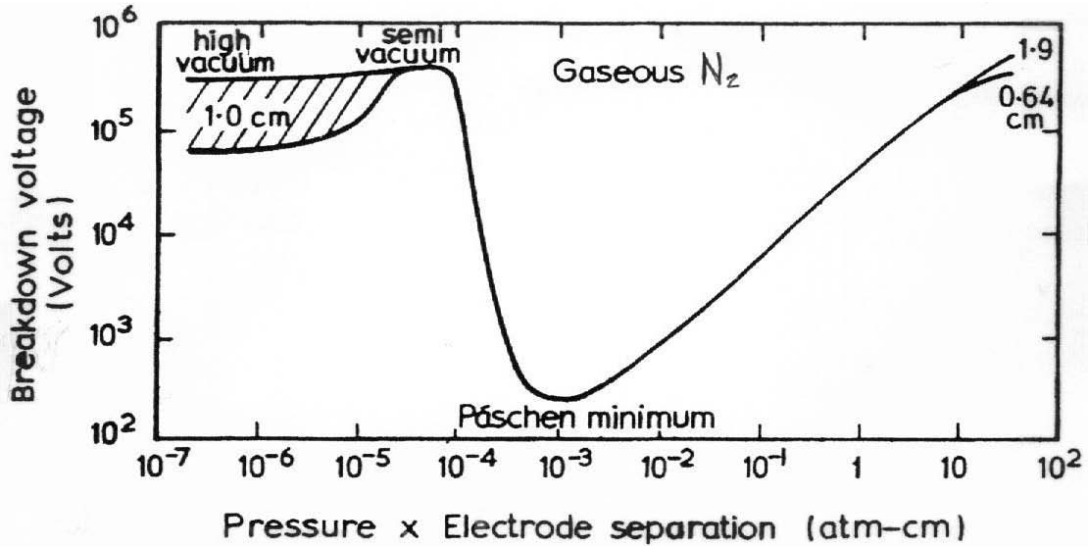
- Paschen curve doesn’t go to high vacuum
- How does Paschen help us?
  - We test high HV PCBs in air before going to vacuum
  - Breakdown V in air is lower than in vacuum
  - Gas trapped in voids of bulk insulator material are governed by it
  - If unit is to operate through Paschen minimum
    - We are warned of hazard

Extending the Paschen Curve, p1

- High vacuum
  - Pressure is too low for gas ionization
  - Reduced background gas load remains
    - Clean vacuum systems: mostly H_2O, some N_2, O_2, CO_2, etc
    - In our systems, also various outgassing products from HV materials
      - Un-polymerized monomers, various solvents, etc
  - Oxidation layers develop very fast in high vacuum
    - On clean metals
    - In seconds or faster for some metals
    - Even “noble metals” form a thin layer of oxides or ionic complexes
  - Partial discharge currents still develop with high voltage
    - Emitted electron pulses
    - From cathode
  - Photons are emitted from anode
    - Where emitted electrons strike
      - Pumping energy back into emission zone

Extending the Paschen Curve, p2

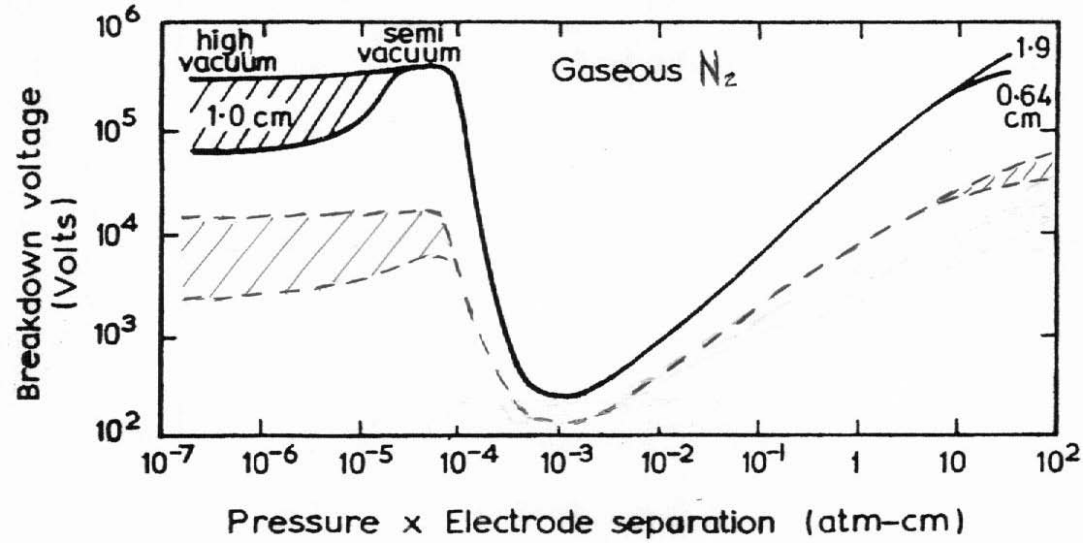
- High Vacuum (continued)
  - Multiple complex emission processes combine at Cathode, from
    - Sharp metallic µ-projections
      - Mechanism applies only at extremely high fields
    - Zones of non-metallic surface – mostly oxides, µ-projections
    - Adsorbates
    - Particulates, dust: metallic and non-metallic



From C. M. Cook & A. H. Cookson, IEEE Trans., E1-13, Aug 1978

Extending the Paschen Curve, p3

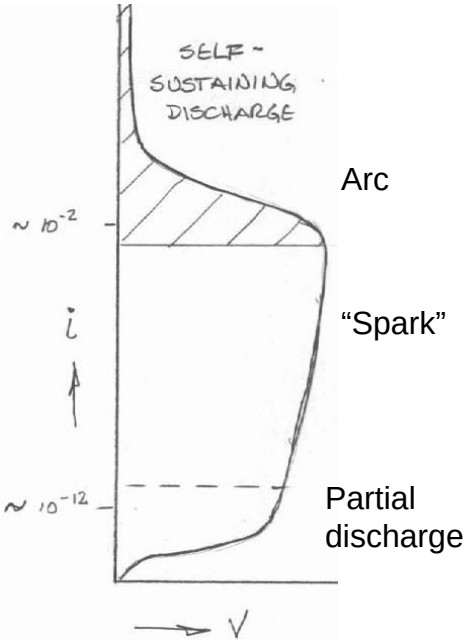
- Can we use the extended Paschen curve for design?
  - NO
- Doesn't include
  - Distance dependencies
  - Geometry induced field intensifications
  - Dielectrics, etc



Hypothetical design curve for realistic geometry and conditions (lower dashed curve)

Stages of Breakdown, p1

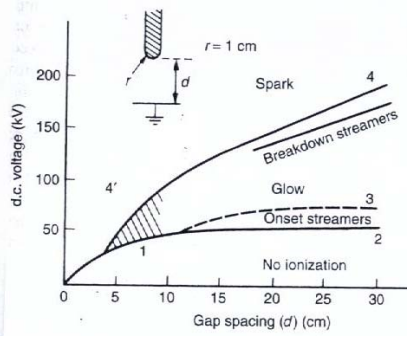
- Partial discharge - Summary
  - Pre run-away condition: charge bursts
  - Essential conditions
    - Sufficient electric fields
    - Initiating electron(s) leading to avalanches
    - Source of gas molecules
    - Feedback mechanisms
      - » UV photons
      - » Energetic ions
      - » Heat, releasing more gas and electrons
      - » High, irregular electric fields from avalanche charges
      - » Some dependence on cathode material
  - Generally persists only when d ≤ 5 mm and P ≤ 1 std atm



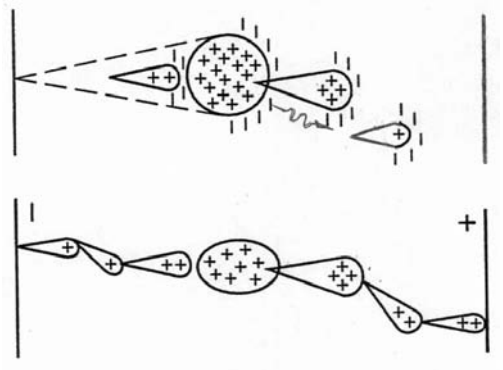
Over-simplified plot of discharge-spark-arc i-V plot.

Stages of Breakdown, p2

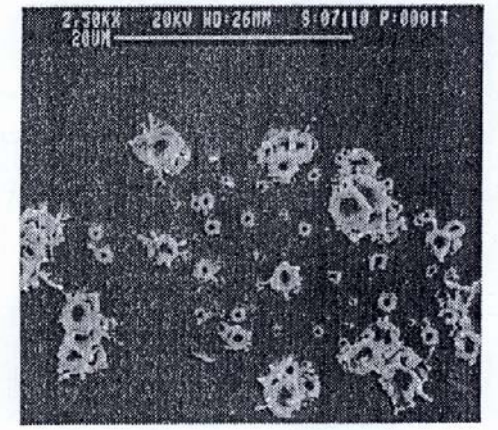
- "Sparks"
  - Multiple avalanches coalescing to produce streamers
  - Typically at higher pressures and larger gaps
  - May involve contaminant particles
    - Are electrically charged and become projectiles
    - Strike opposite electrode producing vapor and more projectiles, etc
  - Tend to pit conductors
  - Usually quench rapidly



More detailed diagram of various forms of breakdown; From Kuffel, Zaengl and Kuffel



Avalanches (a) becoming streamers (b); From Kreuger



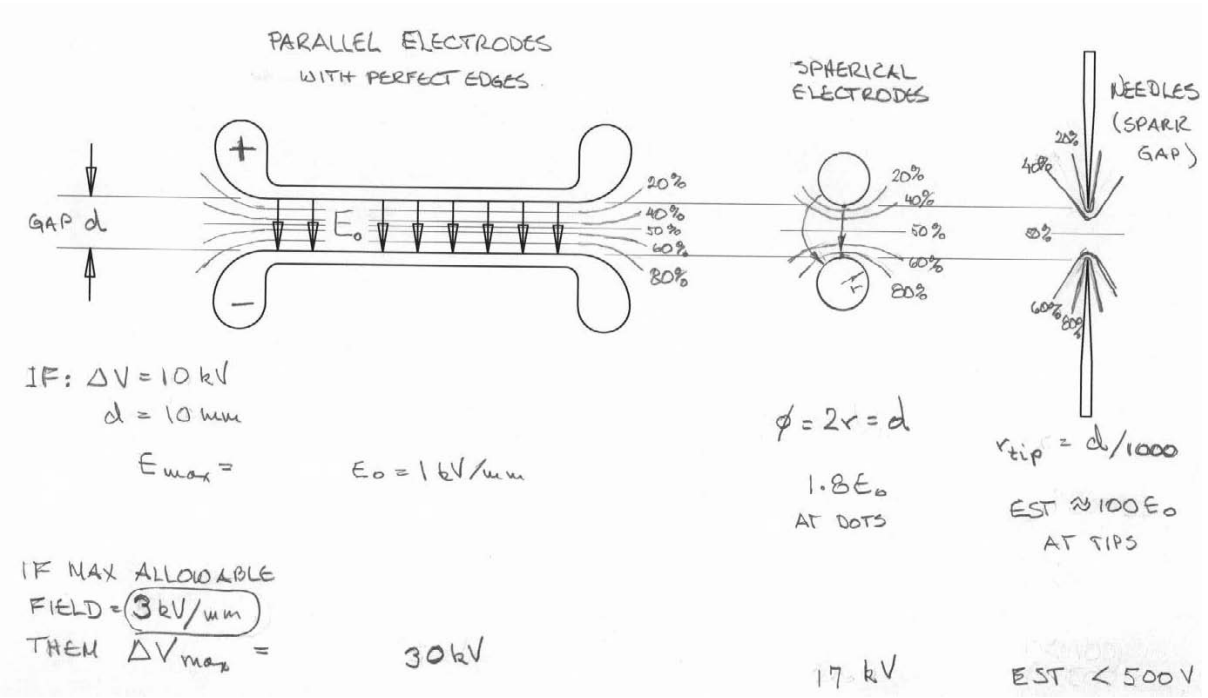
Electrode cratering from a spark; Photo from Latham

Stages of Breakdown, p3

- Arcs
  - Plasma tube develops:
    - i↑, Ω way↓, sustaining V↓
  - 5,000 to 20,000 °C
  - One author claims up to 10^8 A/cm^2
  - Often hard to quench
    - Feed off of electrode material

Geometry and electric fields, p1

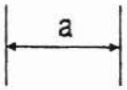
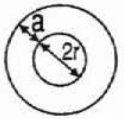
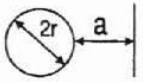
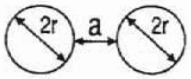
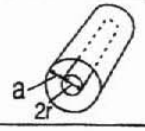
- Distribution of potential energy around conductive electrodes
  - Continuoum of potentials
- Entirely geometry dependent



Geometry cannot be ignored!

Geometry and electric fields, p2

Max fields for convenient geometries

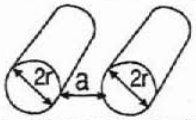
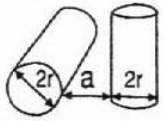
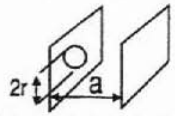
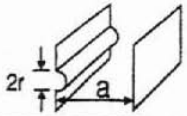
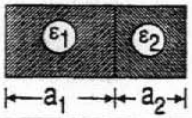
Configuration		Formula for E_{MAX}
Two Parallel Plane Plates		$\frac{U}{a}$
Two Concentric Spheres		$\frac{U}{a}\left(\frac{r+a}{r}\right)$
Sphere and Plane Plate		$0.9\,\frac{U}{a}\left(\frac{r+a}{r}\right)$
Two Spheres at a Distance from Each Other		$0.9\,\frac{U}{a}\left(\frac{r+a/2}{r}\right)$
Two Coaxial Cylinders		$\frac{U}{2.3\ r\ \lg\left(\frac{r+a}{r}\right)}$
Cylinder Parallel to Plane Plate		$0.9\ \frac{U}{2.3\ r\ \lg\left(\frac{r+a}{r}\right)}$

Notes:
1. Units: Volts & cm
2. $\lg = \log_{10}$
3. Factor 2.3 = $\ln(C)/\log_{10}(C)$

See website: [http://www.nessengr.com/techdata/fields/field.html] for field solver of these geometries.

Geometry and electric fields, p3

Max fields for convenient geometries, continued

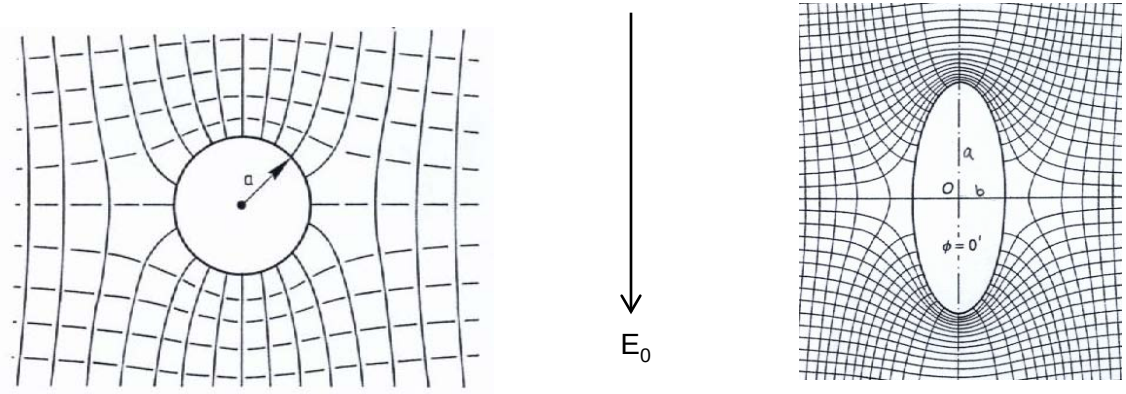
Cylinder Parallel to Plane Plate		$0.9\ \frac{U}{2.3\ r\ \lg\left(\frac{r+a}{r}\right)}$
Two Parallel Cylinders		$0.9\ \frac{U/2}{2.3\ r\ \lg\left(\frac{r+a/2}{r}\right)}$
Two Perpendicular Cylinders		$0.9\ \frac{U/2}{2.3\ r\ \lg\left(\frac{r+a/2}{r}\right)}$
Hemisphere On One of Two Parallel Plane Plates		$\frac{3U}{a}$; (a >>r)
Semicylinder On One of Two Parallel Plane Plates		$\frac{2U}{a}$; (a >>r)
Two Dielectrics Between Plane Plates		$\frac{U\,\varepsilon_{MAX}}{a_1\ \varepsilon_2 + a_2\ \varepsilon_1}$ E_{MAX} OCCURS IN BODE OF E_{MIN}

See notes on previous page

These results mostly exceed those for realistic geometries - handy for upper limits

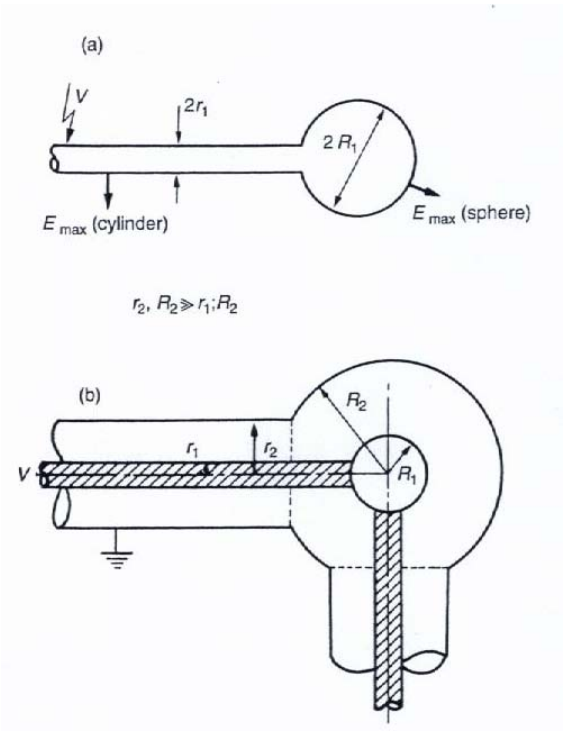
Geometry and electric fields, p4

- Conductors in parallel field gas or vacuum gap
  - Conductor size << gap
  - $\varepsilon_{gap} = 1$
  - Field intensifications:
    - Sphere $E_{max} = 3 \times E_0$
    - Rod $E_{max} = 2 \times E_0$
    - Ellipsoid (aligned with E0), $E_{max} >> E_0$



Geometry and electric fields, p5

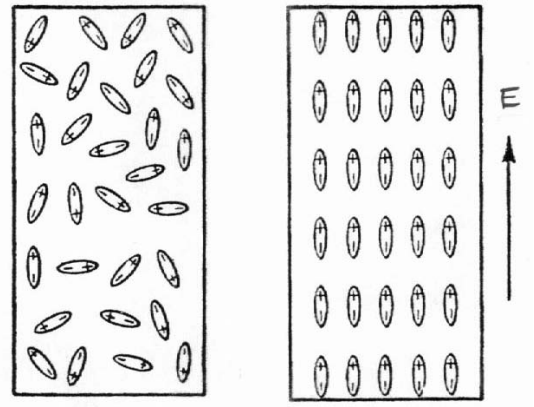
- Wire bends intensify fields
- Use balls and rods having uniform surrounding electric fields



Constant field HV rod and ball hardware

Dielectrics, p1

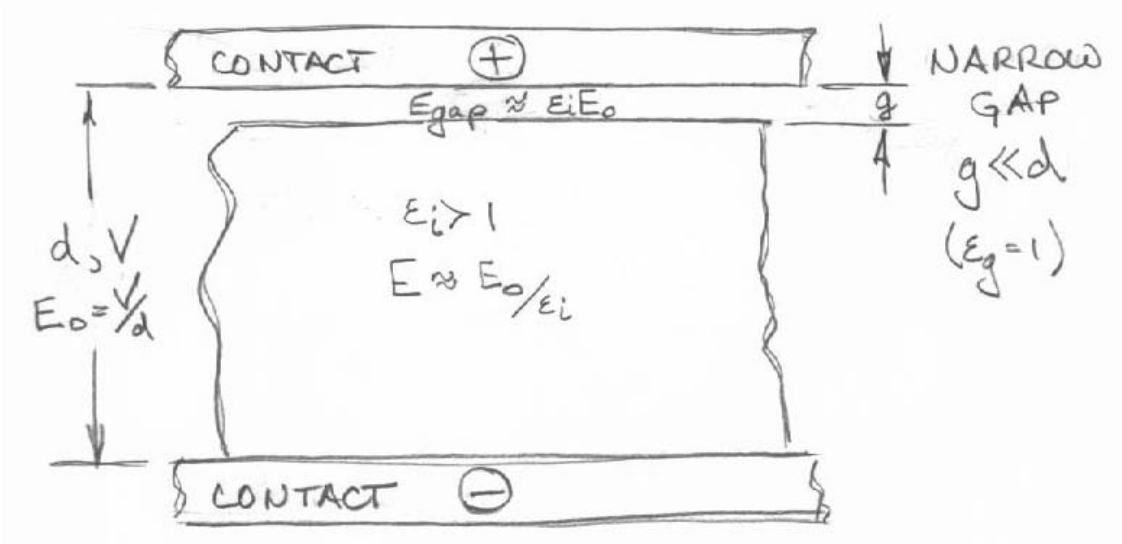
- Dielectrics
  - Materials whose atomic dipoles can be aligned by the forces of an electric field
    - Called displacement charges
  - Degree of susceptibility is called permittivity or relative dielectric constant, ε
    - $\varepsilon_{air} = \varepsilon_{vac} = 1$
    - $\varepsilon_{insulator}$ = typically 2 to 12 (some glasses to ~30)



Schematic of displacement dipoles in an insulator un-polarized (left) and umpolarized (right). From Introduction to Electric Fields by Walter E Rogers, 1954.

Dielectrics, p2

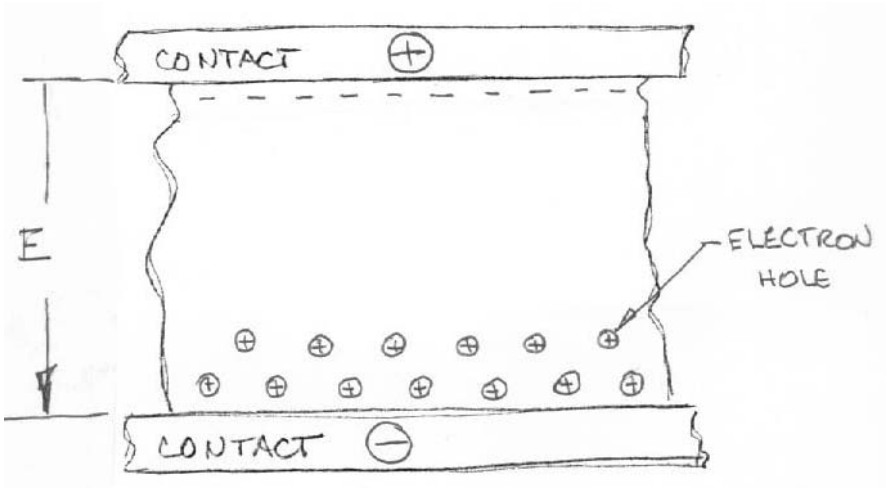
- Multiple dielectrics
- One solid and one gas dielectric
  - Displacement dipoles in dielectric
    - Reduce $E_{dielectric}$ x ε_i
    - Increase E_{gap} x ε_i



Picture

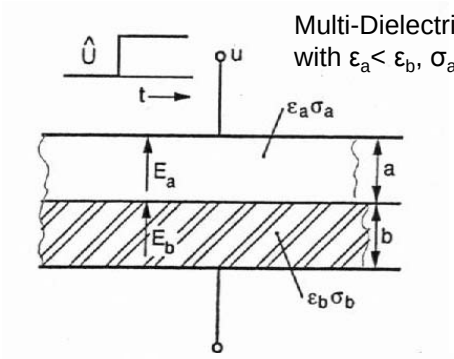
Dielectrics, p3

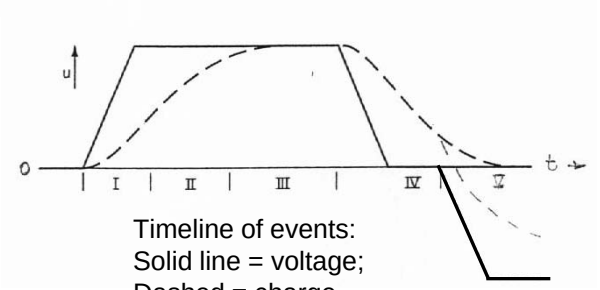
- Dielectric Space Charge - DC
  - Electrons and holes are mobile
    - Not ions
    - Settling times depend on insulator bulk resistivity, σ_i, capacitance and geometry
    - V Polarity reversal can damage dielectric



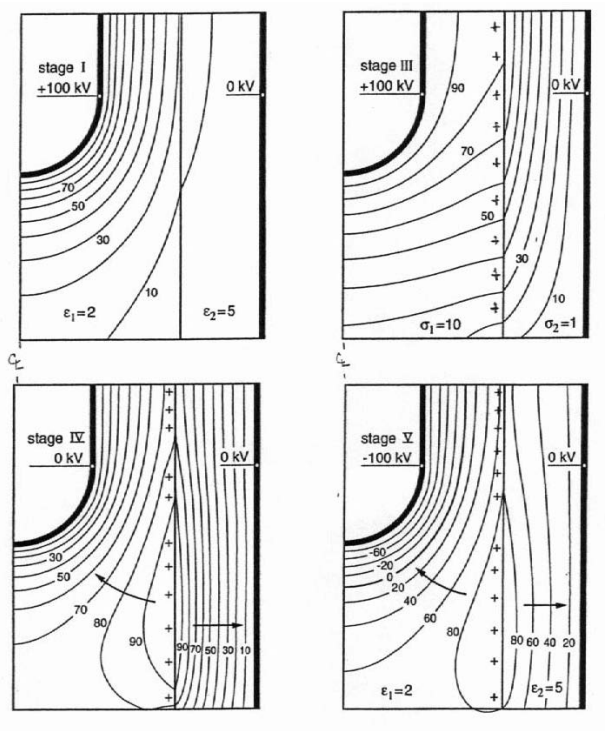
Dielectrics, p4

- Multi-layer dielectrics
  - Great benefits and potential hazards
    - The end of a radiused center conductor in a grounded coaxial shell
    - Two dielectrics





- Can overstress dielectric



Field plots for four stages on timeline; field contours are 10 kV except for stage V; represent figures of revolution about centerlines (CL).

Contours
20 kV/line

Plots from Kreuger

Dielectrics, p5

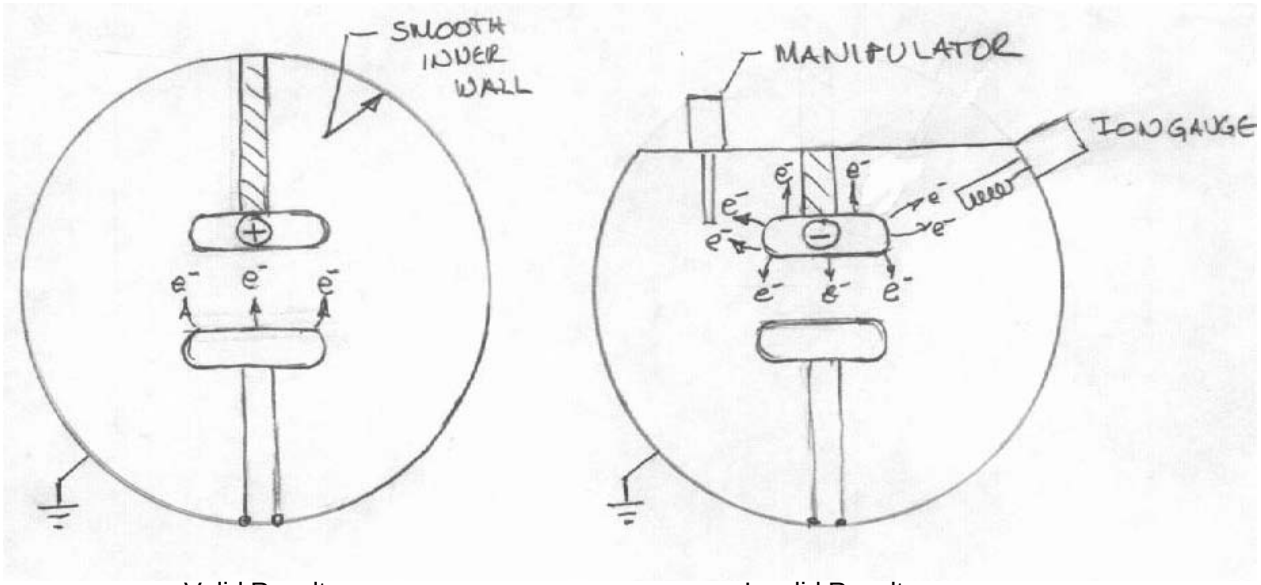
- DC Electric Fields with
  - No solid dielectric
    - Depend on conductor geometry only
  - Single solid dielectric filling field
    - Depend on bulk insulator dielectric constants, ε_i and conductor geometry
  - Multiple solid dielectrics filling field
    - Depends on ε_i's, bulk insulator resistivities(σ_i) and geometry
    - Settling time constants at dielectric interfaces may be long
      - In the order of hours to a day
  - Solid dielectric plus gas dielectric
    - Depends on ε_i's and σ_i, insulator surface resistivity (ρ_i) and geometry
      - ρ_i is often << σ_i
      - Due to adsorbates, contaminants, etc
      - Resistance = resistivity x area factor
        - » Area factor = (conductance path length) / (conductive area) = L/A

Reality

- In a perfect world:
  - Perfect: parallel electrodes, surface smoothness, cleanliness, etc
  - Electron emission field = 10^6 to10^7 V/mm
    - 1000 to10^4 kV/mm
      - kV/mm is unit of electric field used hereafter
    - Lifts a conduction band electron from its molecule into vacuum
      - Overcomes inter-atomic electric fields
- Real life in a conservatively designed unit:
  - 1 to 3 kV/mm will generally avoid breakdown
  - 10 kV/mm is very risky

Testing, p1

- If you test
  - Don’t let the chamber participate
  - Use +HV if possible (V < 20 kV)

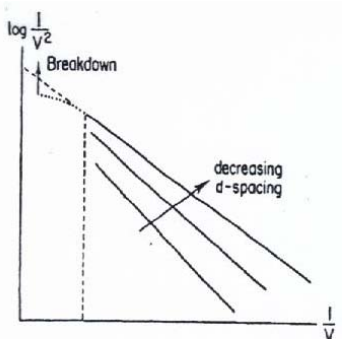


Valid Results

Invalid Results

Testing, p2

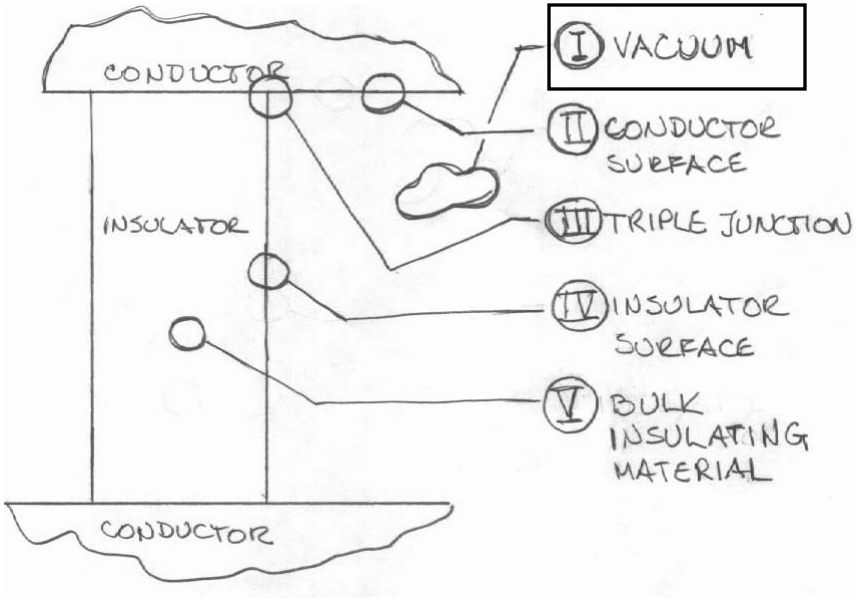
- Sensing Discharge
  - Detection
    - CCD camera in a darkened room
    - Discharge noise pickup
      - Sometimes sound
  - Measurement
    - Sensitive charge pulse sensing equipment
      - Measure rate & pulse height distribution of charge pulses
        - » Order of peco-Coulombs thresholds
    - Fowler-Nordheim plots
      - Not applicable in presence of oxides
        - » Applicable on clean contacts only
        - » At extremely high voltages
      - Probably not useful
  - During diagnostic tests
    - Time constants reveal important clues



Fowler-Nordheim Plot
From Latham

Practical Design Considerations

I. “Vacuum”, p1


CONDUCTOR
INSULATOR
CONDUCTOR
I VACUUM
II CONDUCTOR SURFACE
III TRIPLE JUNCTION
IV INSULATOR SURFACE
V BULK INSULATING MATERIAL

“Vacuum”, p2

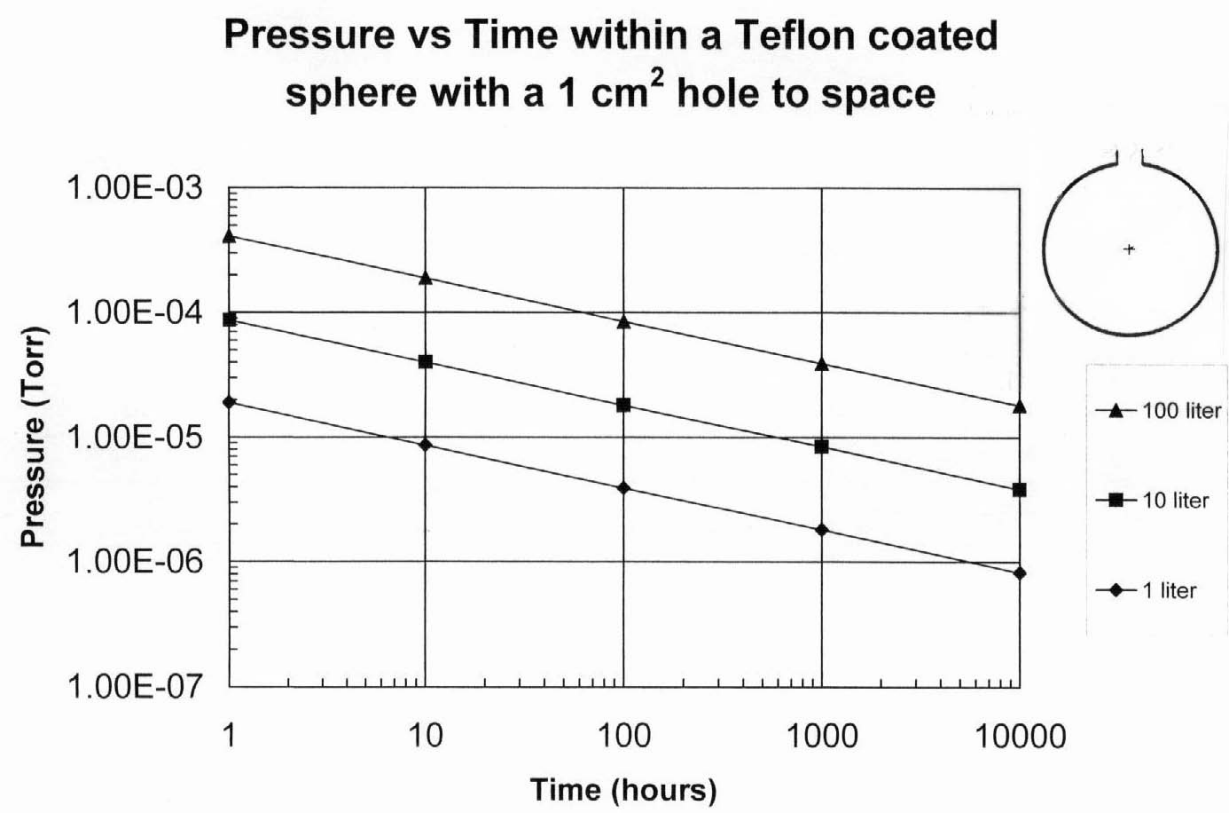
- Measure of vacuum:
  - Traditional: 1 Torr = 1 mm Hg = 1/760 std atm = 1.3×10^{-3} std atm
  - More recently: 1 bar = .99 std atm

Chart from Roth

Condition	Pressure		Mean Free Path	Gas Density
	Torr	= Atm	(λ)	(mol/cc)
Atm at STP	760	1	67 nm	2.5×10^{19}
Part. Vac	1	1.3×10^{-3}	51 μm	3.3×10^{16}
Poor Vac	10^{-3}	1.3×10^{-6}	51 mm	3.3×10^{13}
Fair Vac	10^{-6}	1.3×10^{-9}	51 m	3.3×10^{10}
Good Vac	10^{-9}	1.3×10^{-12}	51 km	3.3×10^{7}
Space Near Earth	10^{-15}	1.3×10^{-18}	5×10^{6} km	30

- Electronics box pressure after several months on orbit?
  - Not known, to my knowledge
  - Many material outgassing contributions
  - My estimated electronics package pressure is10^{-5} to 10^{-8} T
  - Usually inside spacecraft and thermal blankets (MLI)
  - Warmer temperatures augment gas release

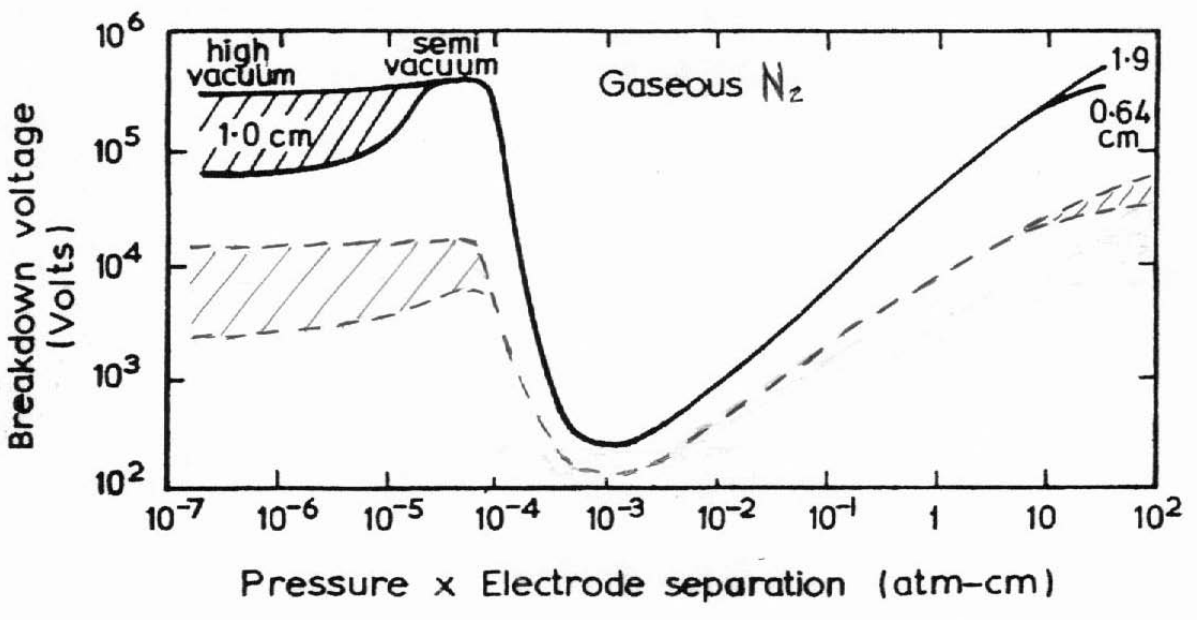
“Vacuum”, p3



Calculated pressure inside an outgassing Teflon sphere based on best available outgassing rate data for Teflon (Tom Sanders)

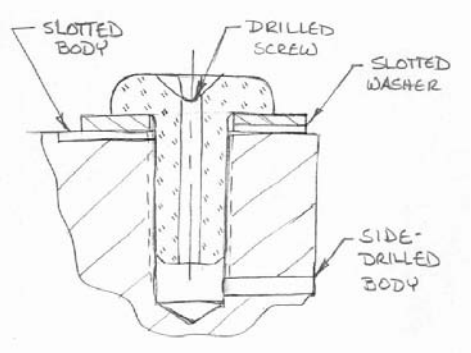
“Vacuum”, p4

- Good news:
  - Always good enough vacuum for electronics
- Bad news:
  - Never really high enough vacuum for many detectors

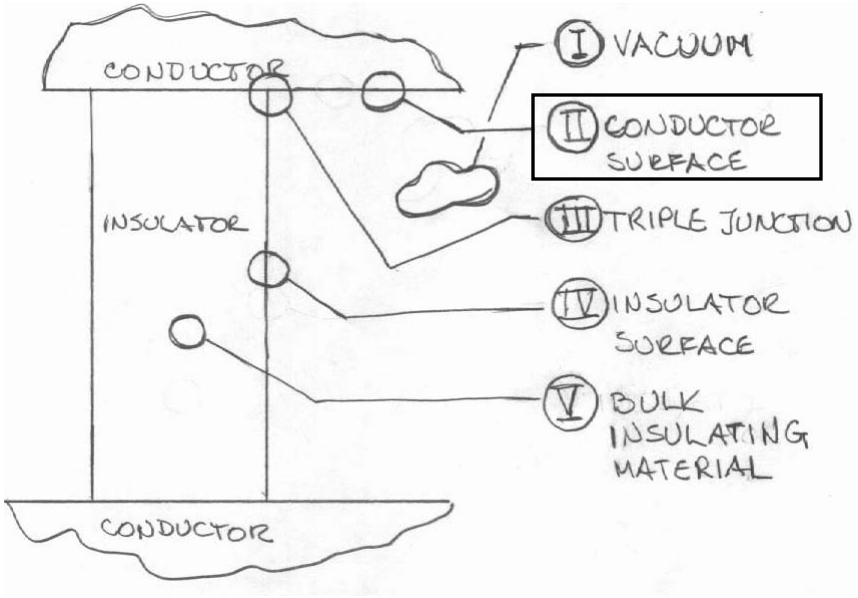


“Vacuum”, p5

- Good practice
  - Design for good enclosure venting
    - Long time rule:
      - 1 square inch vent area per cubic foot of volume
        - » Volume / Area ≤ 1730 inches
      - Sometimes given as: Vol / Area ≤ 2000 inches
    - Vent away from sensitive instrumentation, if possible
      - And vice versa
  - Block external EUV
  - Vent all trapped volumes
    - Especially below blind screws
    - Most threads do not plug gas passage
    - Virtual leaks delay ground testing
  - Vacuum pre-bake all assembled units
  - Strive for extreme cleanliness
    - Particulate
    - Chemical
      - Often called “non-volatile residue” (NVR) (=> leads to complacency)
      - Hazardous because it IS volatile in flight environment



II. Conductor Surfaces, p1

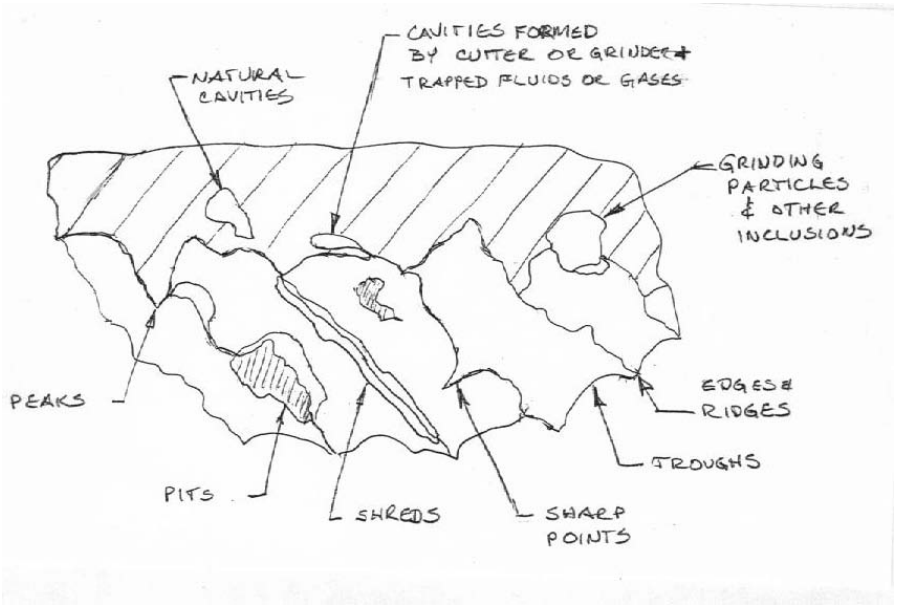


Conductor Surfaces, p2

- Material choice is limited by practicality in electronics
- Optimal conductor materials
  - Low outgassing
    - With benign outgassed volatiles
  - Less prone to oxidation
  - Carefully cleaned
    - Solder rosins, trace plating solution residues and masking materials
    - Sometimes conformal coatings
- Control conductor surface smoothness
  - Smoother is better
  - Smooth solder applications
    - Especially solder spikes

Conductor Surfaces, p3

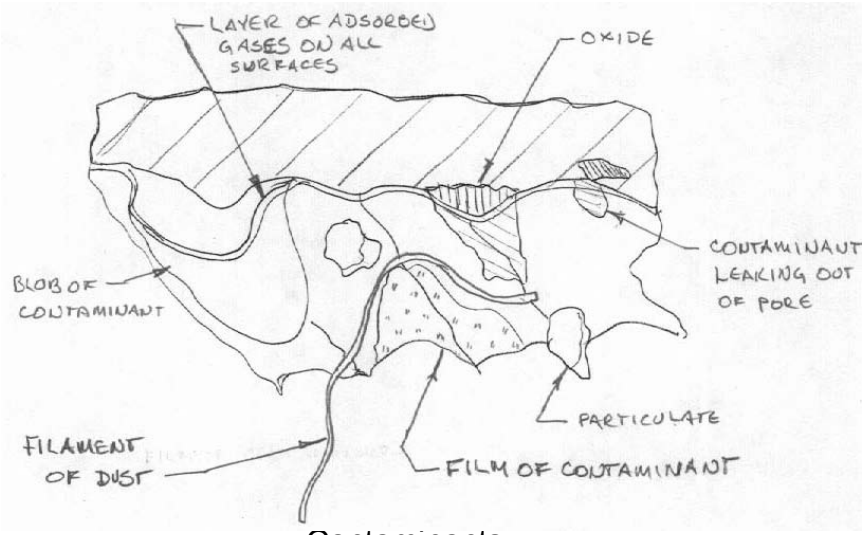
- Surface smoothness near HV
  - Nearly all manufacturing methods produce microscopic roughness
  - Ridges, troughs, spikes, pockets smeared closed, fragments, shreds



Microscopic machined features

Conductor Surfaces, p4

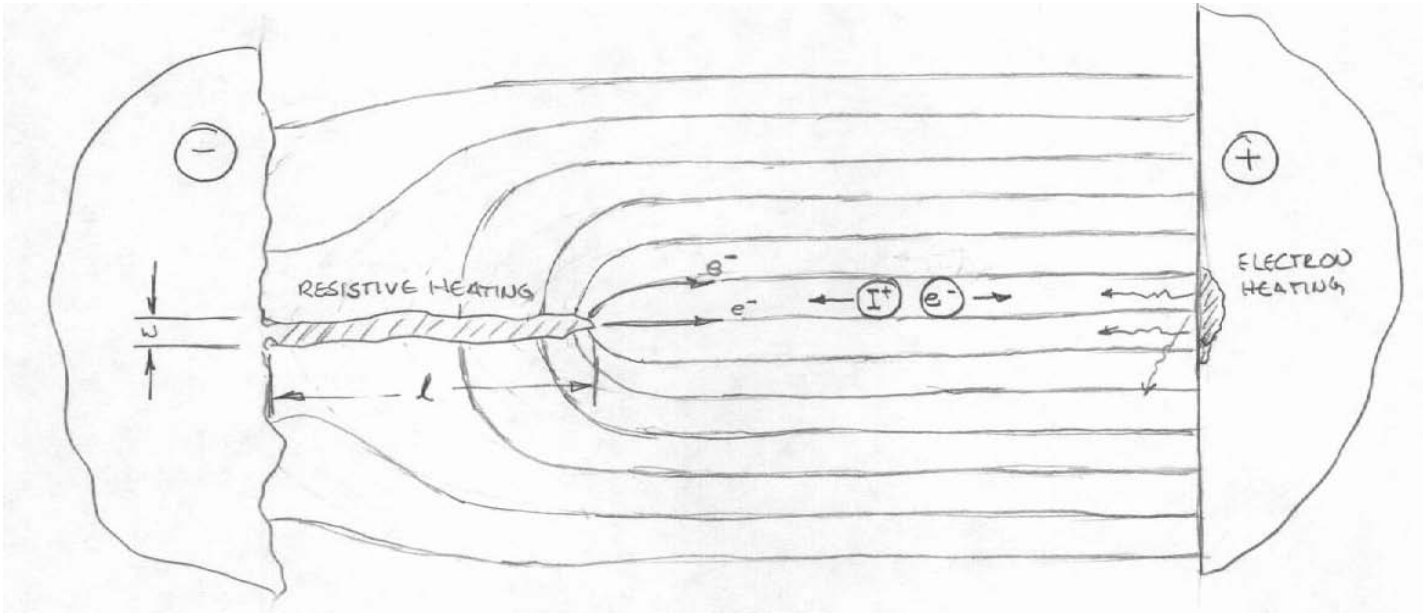
- Surface Cleanliness
  - Oxidation
  - Particulates
  - Chemical contaminants
  - Adsorbed gases
    - Mono-layer adsorption time at 10^{-6} T: secs!
  - Cavities trap cutting oils, fluxes, cleaning fluids, other contaminants



Contaminants

Conductor Surfaces, p5

- Fibers and shreds
  - electric attraction lifts them into fields
    - Field amplification factors: 10s to 100s



Electric force lifts shred or fiber into field gap producing highly intensified fields at the tip , elevated e^- emission, resistive heating in shred, photon emission, etc.

Conductor Surfaces, p6

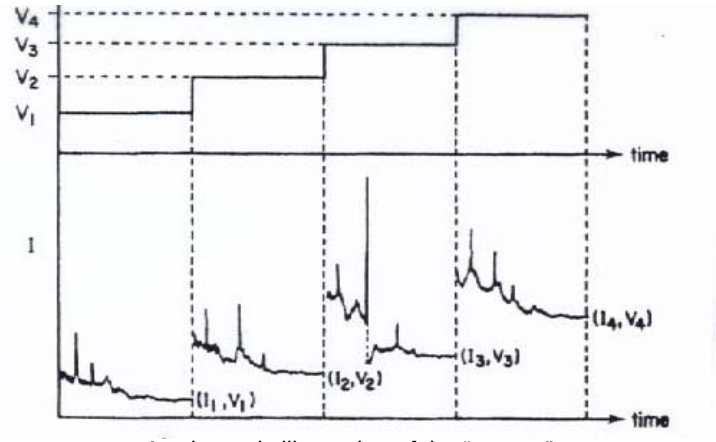
- Mitigations
  - Polish surfaces, mechanically and/or chemically
    - Both methods together are best
  - Smooth solder balls at terminals
  - Electro-plate contacts
    - Ni + Gold
    - Strive for particle-free plating baths
      - » Particles can add roughness to plated surfaces
  - Radius corners and edges generously
  - Follow best cleanliness practice

Conductor Surfaces, p7

- Thermal Sensitivity
  - Warmed surfaces release
    - Adsorbed gas
    - Gasses from micro cracks and cavities

Conductor Surfaces, p8

- "Conditioning" of un-coated HV conductors
  - Apply HV to burn off limiting protrusions, dust, etc
    - Requires high current lab power supplies
    - See
      - Latham, pp 33-39
      - Arora & Mosch, p 267
      - Practice in advance is advised
  - Effective but carries risk
  - After removal from vacuum
    - Some benefit is lost
      - Fresh dust, corrosion, etc
- Not appropriate for coated terminals

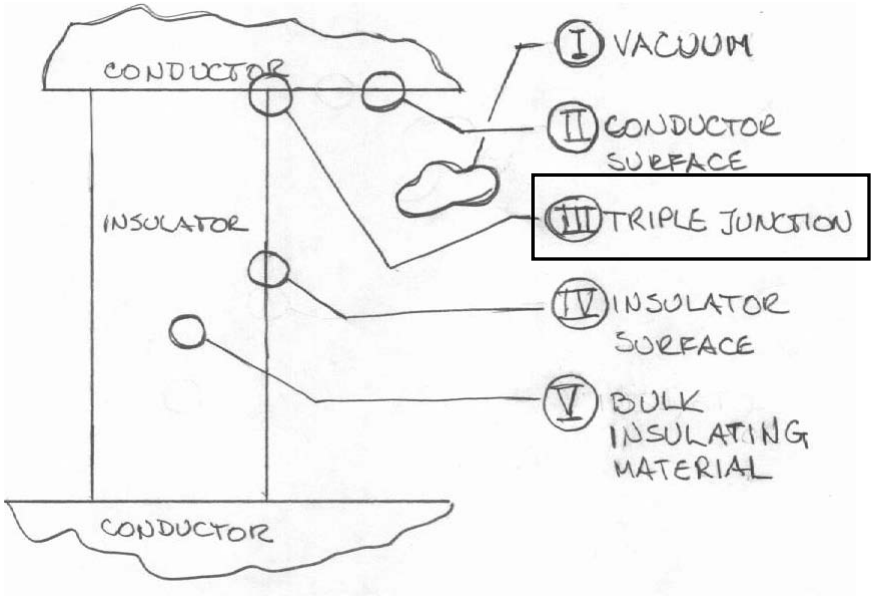


A schematic illustration of the "current" conditioning method, from Latham

Conductor Surfaces, p9

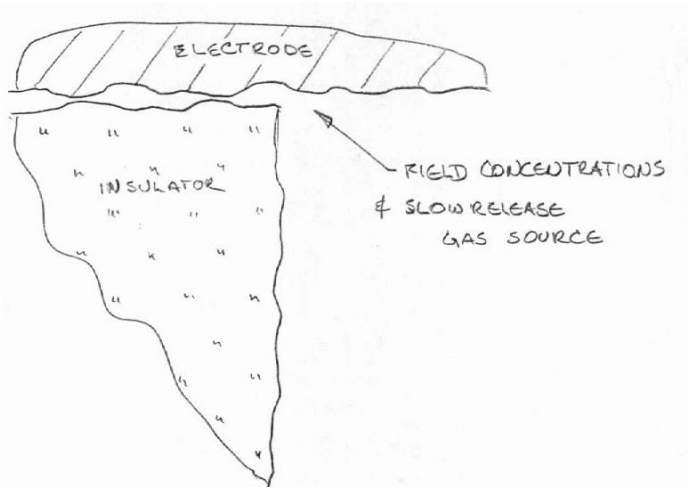
- Thin dielectric coating on conductors
  - Cab be good discharge suppression barrier
    - Excludes moisture
    - Polyurethane PCB coatings
      - Often used; various issues
    - Paralene C
      - Higher dielectric strength
      - Good outgassing
      - Excellent penetration into cavities (e.g. under components)
      - Good coverage uniformity
      - Difficult to clean off connector contacts
    - Nuisance to make repairs through
    - Higher outgassing with raised temperature

III. Triple junctions, p1



Triple junctions, p2

- Definition: Zone where a conductor, an insulator and a gas dielectric or vacuum come together
  - Microscopic irregularities at mating surfaces
    - Trap gas for abundant, slow release
    - Enhance local electric fields
  - Local warming boosts
    - Field emission
    - Further gas release
- Ignition points for discharges



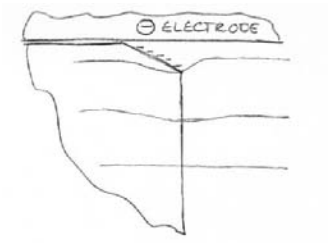
Microscopic view of triple junction

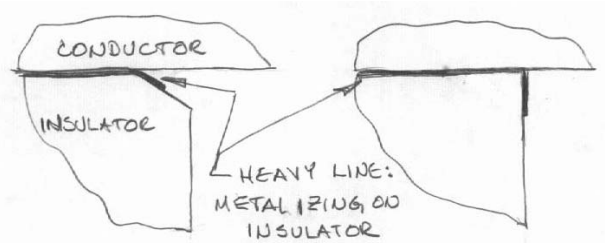
- Essential to control!

Triple junctions, p3

– Mitigations:

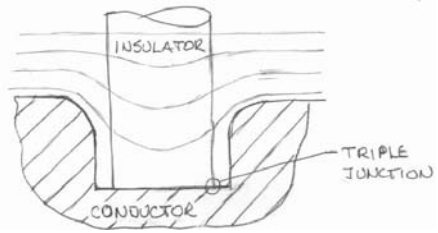
- Chamfer ends lightly per Wetzer and Wouters
  - Chamfered edge of insulator becomes charged by high fields
  - Acts to deflect and smooth equipotentials
- Metalize insulator surfaces where they will contact electrodes
  - Ceramics: fired on coatings
  - Polymers: electroplated treatments
- Best: place triple junctions away from high fields



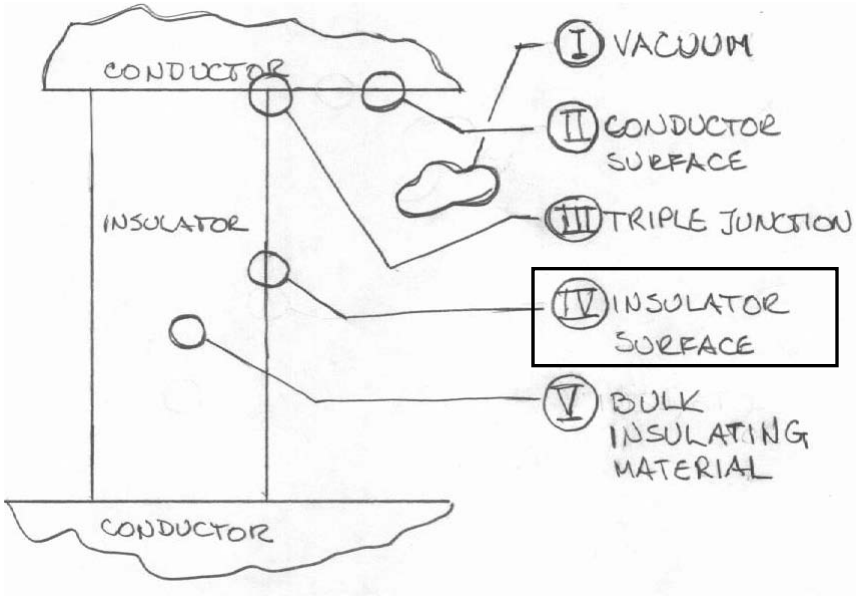


Yes: Chamfered, partially metalized

No: Do not metalized down edge



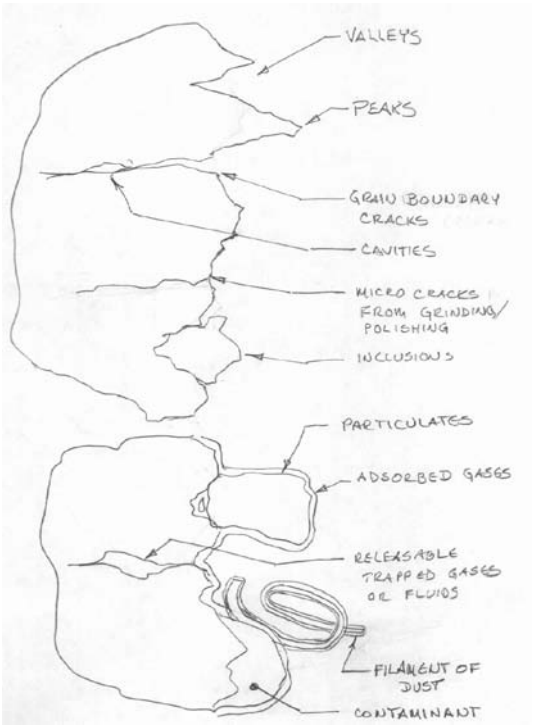
IV. Insulator Surfaces, p1



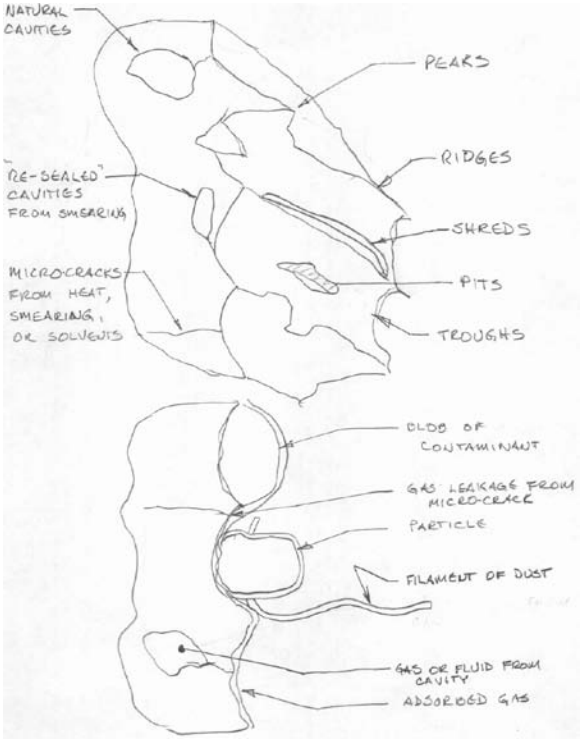
Insulator surfaces, p2

- Surface blemishes : same as in metal manufacturing:
  - Ceramics - ground
    - Peaks, valleys, surface micro cracks, cavities
    - Ceramic, metallic and grinding wheel particles, etc.
      - Acid bath removes all metallics
      - Requires re-firing to remove acid from porosity
  - Engineering plastics - turned
    - Smearing, tearing, shreds & cavities
  - Molded or bonded parts
    - Entrained bubbles, surface smearing and mold shreds
      - Puncture bubbles where visible
  - Bonded Insulator joints
    - Tiny bubbles – breakdown initiation sources
  - Annealing can foster micro-fracture healing
    - In ceramics and plastics
- Contaminants : similar to metal parts

Insulator surfaces, p3



Ceramic surface viewed microscopically, physical features above, contaminants below.



Plastic surface viewed microscopically, physical features above, contaminants below.

Insulator surfaces, p4

- Discharge can occur along insulator surfaces
  - Gas sources, field intensifications are present
  - Surface discharge can be self-sustaining
- Damage from HV discharge
  - To ceramic and polymeric surfaces
    - Discharge can sputter metal onto insulator surfaces
      - Reduces surface resistance unevenly
      - Hence HV standoff V
  - To bare metallic surfaces
    - Discharge can sputter polymers onto conductors
  - On polymeric surfaces:
    - Discharge may char the plastic surface, leaving a carbon track that partially shorts the insulator end to end
      - If possible, select the polymer for high tracking resistance

Insulator surfaces, p5

- Surface charging is dynamic:
  - Charge sprays around, coating some insulator surfaces
  - Alters electric fields
  - New fields redirect sprayed charge, charging different areas
  - Charge leaks off at varying rates
  - Time constants often in order of seconds

Insulator surfaces, p6

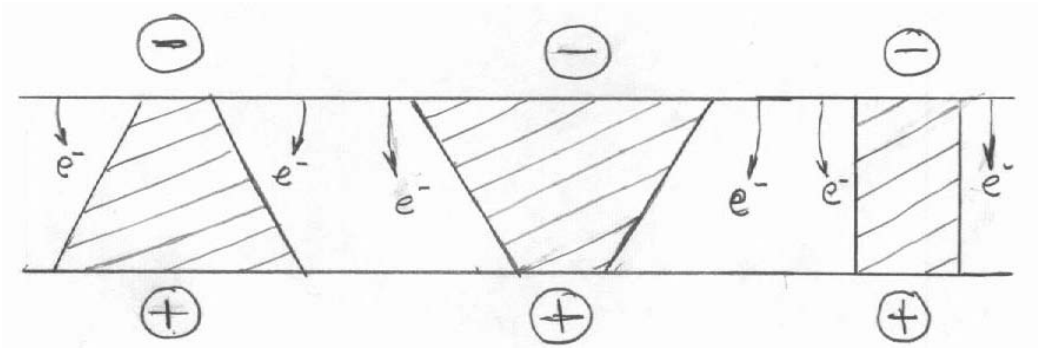
- Thermal effects
  - 2 heating modes
    - Conductive heating of conductors and insulators
      - Small temperature Δ's
      - Slow
    - Discharge heating of surfaces
      - Large transient temperature Δ's
      - Fast
  - Warming causes gas release from surfaces
    - Higher local pressure
    - Points can contribute thermal emission
  - Surface resistivity drops with temperature rise

Insulator surfaces, p7

- Another sub-surface damage mechanism
  - Trapping/De-trapping
    - Theory based in quantum mechanics
    - Purports to explain some breakdown behavior within insulating materials when energetic (>keV) charged particles are implanted
      - Produces sub-surface charge distributions.
    - Dominant cause of damage occurs when charges escape:
      - Releasing intense local heat
      - Causing local mechanical damage
    - See Latham, chapter 9 for more

Insulator surfaces, p8

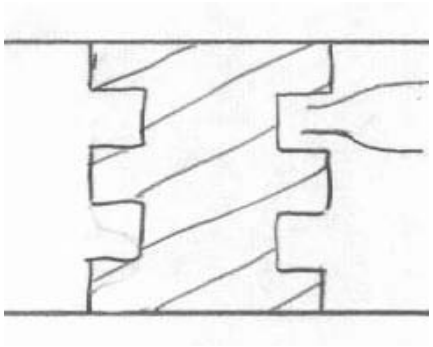
- Insulator shaping
  - Some shapes furnish higher standoff voltages than others
  - Fundamental explanation:
    - Insulator surfaces exposed to direct flows of emitted or breakdown electrons
      - => Lower HV standoff voltages
    - Insulator surfaces shadowed from direct flows of emitted or breakdown electrons
      - => Higher HV standoff voltages



Low HV Standoff V High HV Standoff V Mid HV Standoff V

Insulator surfaces, p9

- Insulator shaping (continued)
  - Extra mass and volume - often impractical
  - See publication by Wetzer and Wouters
  - Convolution: Little harm, little benefit
    - National power distribution system insulators function under entirely different conditions from those in space instrumentation



Insulator surfaces, p10

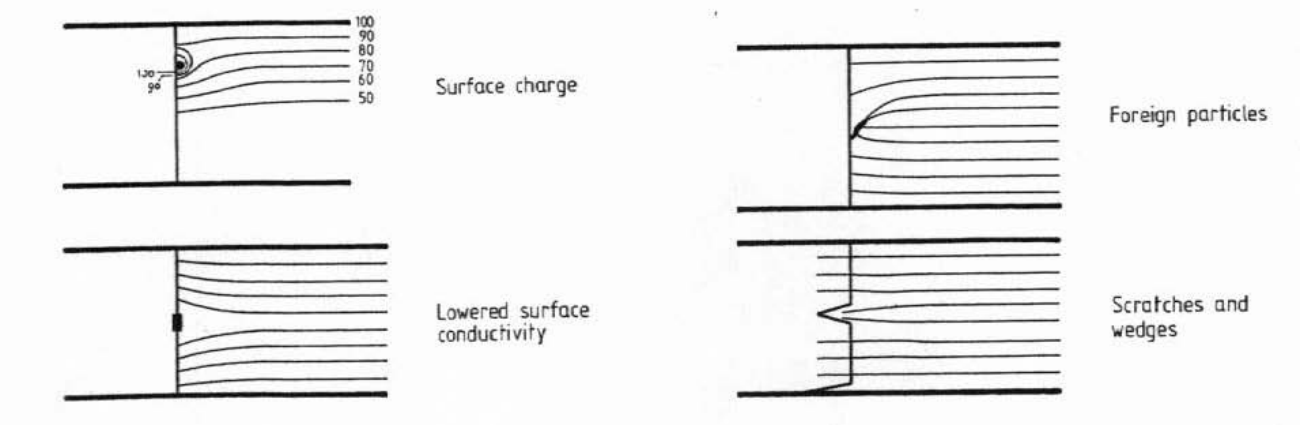
- Handling
  - Ceramic surfaces are harder than metal tools and components
  - Contact with metal will mark ceramics
    - Leaves conductive paths
  - Avoid contact of metal on ceramic insulators
    - At EVERY stage of handling and assembly
    - Use plastic tweezers, containers, etc
  - Glaze surfaces to aid handling and minimize metal marks
    - Caution: improper processing can cause micro-bubbling in glaze
      - Shorts out insulator
      - Demonstrate successful process in advance

Insulator surfaces, p11

- Optimal surface design:
  - Slightly conductive coating on insulators
    - Ω: Order of magnitude ~100's of GΩ/square
      - » High enough not to overload power supplies
      - » Low enough to drain sprayed charge quickly
    - Would produce more uniform fields
      - » Demands good coating uniformity
      - » Some prospective coatings are not thermally stable
    - Still searching for a source
    - Even better : shaped insulators with high, graded ρ
- Possible alternative: slight bulk conductivity
  - Not satisfactory for irregular shapes

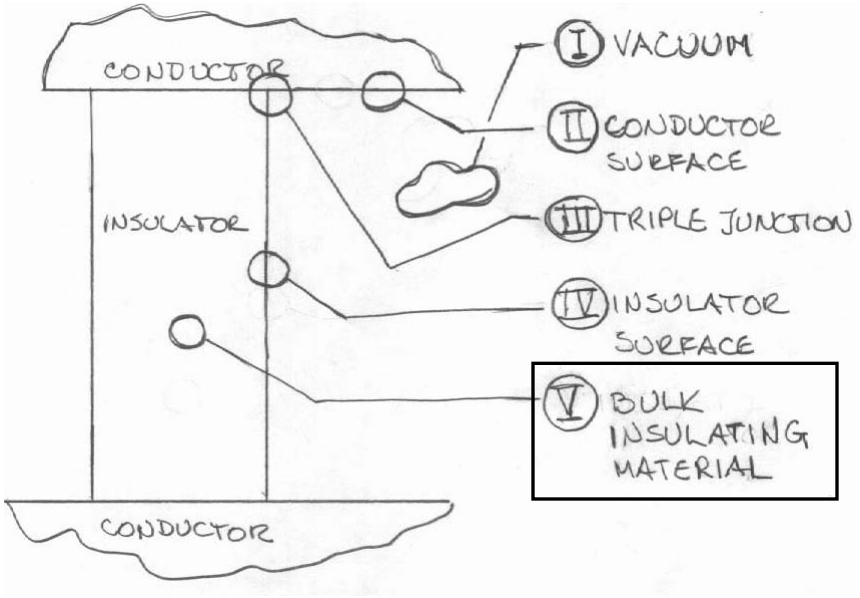
Insulator surfaces, p12

- Field disturbances on insulator surfaces



Plot from Kreuger

V. Bulk Insulating Material, p1



Bulk Insulating Material, p2

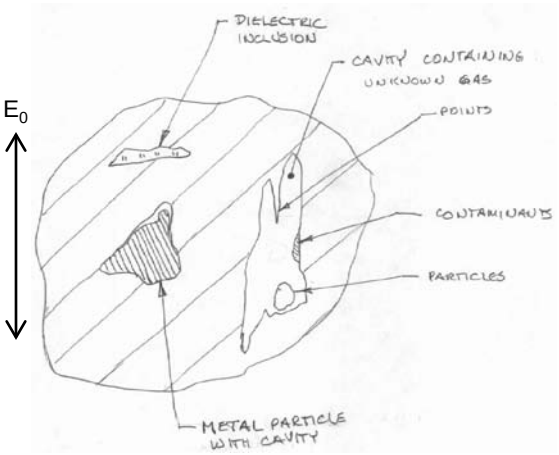
- Three classes
  - Ceramic
    - Usually alumina (Al_2O_3), but many others are available
    - Consolidated from powders under heat and pressure
      - Polycrystaline
      - With glassy components at grain boundarys
      - Always possibility of cavities
    - Mono-crystals: sapphire, other single crystals
  - Engineering plastics
    - Polyimide (Vespel, Kapton), PEEK, Ultem (Polyetherimide), others
      - Relatively low water absorption
    - Teflon & related chloro-fluoro-hydrocarbons
      - Very low water absorption
    - Consolidated from powders under heat and pressure
      - Always possibility of voids
    - Low dielectric noise
  - Molded, laminated, encapsulated and bonded insulators
    - Many materials including epoxies and silicones
    - Laminated PCBs, molded terminals, etc

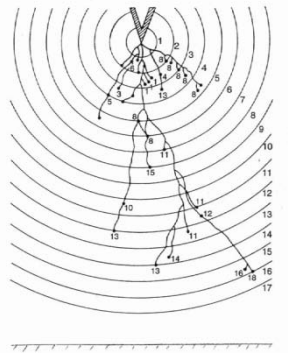
Bulk Insulating Material, p3

- Molded, laminated, encapsulated and bonded materials
  - Usually entrain bubbles
  - Vacuum degassing of liquid compound before curing is ESSENTIAL
  - Laminated systems entrain contaminants along matrix fibers
    - tiny gas bubbles
    - Minute quantities of un- or partially cured polymeric material
  - Risky in higher voltage applications
  - Acceptable bubble size?
    - Depends on field, geometry, ε, etc.
    - Generally very small
    - Impossible to define or eliminate
- Minimize these materials near HV

Bulk Insulating Material, p4

- All insulators have internal flaws
  - Inclusions, cavities, bubbles
    - Frequently cavities form around inclusions
      - Particularly conductive inclusions
      - Aggravated by thermal expansion/contraction
    - Cause high internal fields
      - Especially in cavities perpendicular to field
- Discharge within cavities
  - Enhanced fields
    - Especially if cavity is spiky internally
  - Internal pressure close to atmospheric
    - Increases with temperature
    - May leak slowly
  - Ionic erosion at both polar ends of cavity
    - Directed toward electrodes by fields
  - Causes local heating
  - Chemically active
  - Once started, treeing & burn-through occur rapidly





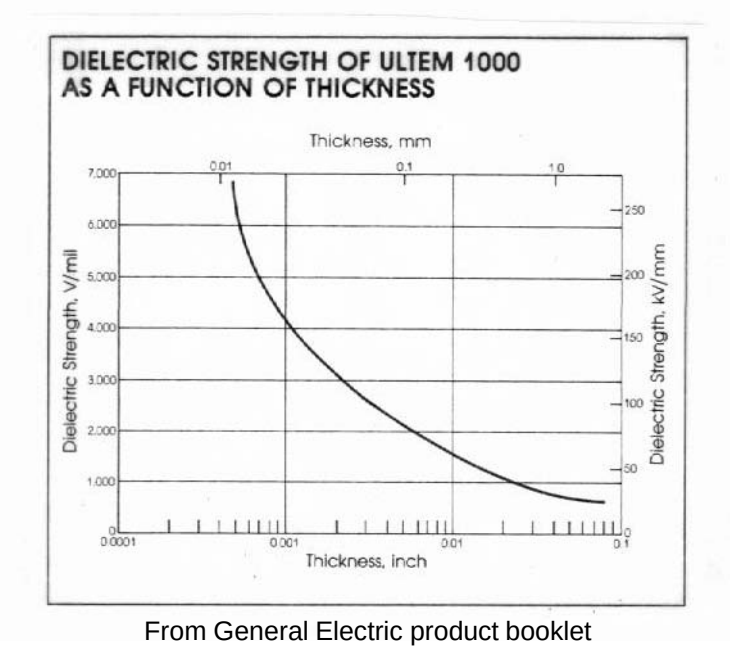
Treeing and near burn-through in plexiglass; from Kuffel, Zaengl & Kuffel

Bulk Insulating Material, p5

- HV standoff V degrades with temperature rise
  - Critical temperature dependent functions
    - Electric material properties
      - ε, σ, DS etc
      - DS, σ and ρ drop sharply
    - Structural material properties
      - Strength, rigidity, plasticity, etc
        - » Weaker, more flexible warm
        - » More brittle cold
      - Gas pressure in voids increases
  - Thermal expansion stresses
    - Internal flaws can creep, separations enlarge
    - May weaken or break insulators
    - Mechanical stress worsens some electronic properties
  - Insulators are all poor thermal conductors
    - Usually sustain gradients
  - High fields warm the insulator

Bulk Insulating Material, p6

- Published Dielectric Strength (DS)
  - BEWARE!
  - Nearly all measurements are per ASTM D149
  - Spec'ed HV stand-off times between 10 and 300 seconds
    - Only 5 minutes max! Way too aggressive for us
  - DS varies inversely with insulator material thickness
    - Spec requires NO correlation to a standard thickness
    - Often inconsistencies among published figures
    - Most insulator suppliers furnish only one DS value
      - Two at most
  - Approximate correction (from Carl J. Tauscher):
  - Derate DS heavily



From General Electric product booklet

$$DS_d = DS_m(t_m/t_d)^{1/2}$$

d = desired

m = measured

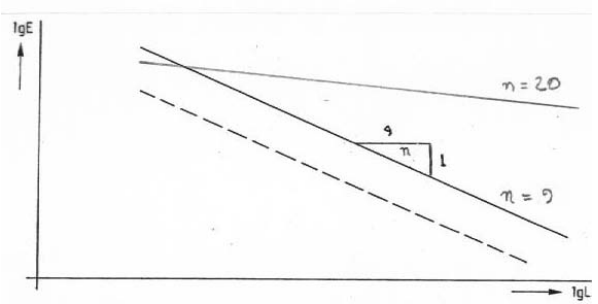
t = thickness

HV System Lifetimes

HV System Life Time, p1

- All HV systems have a limited life
- From the HV cable industry comes the EMPIRICAL relationship:

$$LV^n = C_i$$



  - L = life time
  - V = expected operational voltage
  - C_i = constant, individual to each system
    - NOT a universal constant
  - Exponent n is called Slope on log-log paper
    - Not presented in the conventional fashion
      - Slope is defined here as 9, not -1/9
    - n can vary from well below 9 to as high as 20
    - n = 9 is the generally accepted value for HV cable

HV System Life Time, p2

- Leads to convenient HV test scaling equations:
  - $V_{test} = V_{orbit}(fL_{orbit}/L_{test})^{(1/n)}$

    and
  - $L_{test} = fL_{orbit}(V_{orbit}/V_{test})^{n}$
    - f = the fraction of the orbital lifetime we are willing to expend during the test
- Above equations are simplified:
  - Assume f = only a small fraction of total life
- Bound tests using n = 9 max and n = perhaps 7
  - Use care not to overtest
- LHV test system must be designed for higher voltages than test item
  - Power supplies, connectors, vacuum feed-throughs, cables, grounding
- Use caution

Conservative Rules of Thumb

- Maximum recommended DC design voltages from our experience:
  - Vacuum gaps: 3 kV/mm max; lower is better
  - Along insulator surfaces: 1 kV/mm
  - Within good bulk insulator material: 4 kV/mm
    - Confirm properties – use lower value for thick insulators
  - In atmosphere at STP: 1.5 to 2 kV/mm
    - Up to 3 kv/mm with low humidity
- Max HV turn-on pressure in vacuum:
  - 10^{-5} Torr pressure range
- AC (peak)
  - No experience
  - Would stay below 1/2 of DC values
  - Published AC values range from 0.7 to 0.33 of DC values

Related Topics

Cable, p1

- Cable manufacturers routinely & reliably achieve much higher fields in their dielectrics that we are likely to
  - > 50 years of proprietary development
  - Reynolds shielded HV wire: ~30 kV/mm or more
    - Reliable at rated HV for years
  - Cable makers do things most of us can't:
    - Inner conductor surface ultra-smooth
    - Maximize dielectric purity & density
      - Very few cavities & inclusions
      - Control microscopic gaps between conductors and insulating layers
    - Graduated and/or multiple dielectrics
    - Graduated insulator resistivity adjacent to conductors
    - Sometimes semi-conductor layers
    - Finished wire is HV tested

Cable, p2

- Shielded cable?
  - Shielded cable keeps the field entirely within cable
    - Strongly recommended
    - Fields are uncontrolled at ends where shielding is stripped back
  - Unshielded cable: Exterior fields => pd, etc.
  - Hazard where cable rests on grounded surface
    - Multiple dielectrics, field enhacements
- Cable is damaged when
  - Bent too tightly
    - Dielectric is deformed or separated from conductors
      - Fields are intensified
    - Reynolds shielded cable:
      - Min bend radius = 10 x insulation OD.
  - Less reliable at connector terminations
    - Stripping back shielding creates an air gap => enhances fields
    - Special field shaping ring can help where shield braid is lifted
      - Bubble-free encapsulation

Cable, p3

- Reynolds tests HV wire (2005):
  - At 8.6% of std atmosphere
    - ≈70,000 feet altitude equivalent
    - Near atmospheric Paschen minimum
  - 150% of rated DC voltage, 1 min, shielding grounded
  - AC test (p-p): 70% of rated DC
  - The woven wire shield tested at 3kV AC for 30 sec
    - With respect to a surrounding coaxial ground

Connectors, p1

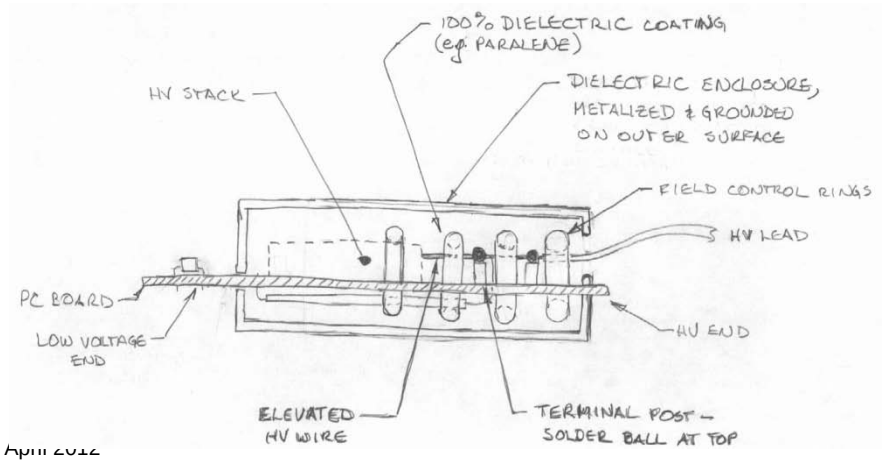
- Commercial HV connectors
  - Ease in making and breaking reliable contact
  - Design options:
    - Hermetically sealed – gas captured in connector
      - O-ring or similar
      - Usually quite reliable, even in vacuum
      - Always risk of slow leakage to Paschen minimum in flight
        - » Breakdown after time
    - Fully vented, labyrinthine breakdown path
  - Controversy about merits
      - Fully vented is better, in my opinion

Connectors, p2

- Screw/lug assembly or captive pin/socked
  - Less convenient, more tiny pieces to drop
  - More labor intensive
  - Most reliable (in my opinion) when properly designed
    - Exposes center conductor fields where shield is stripped back
      - May be an issue

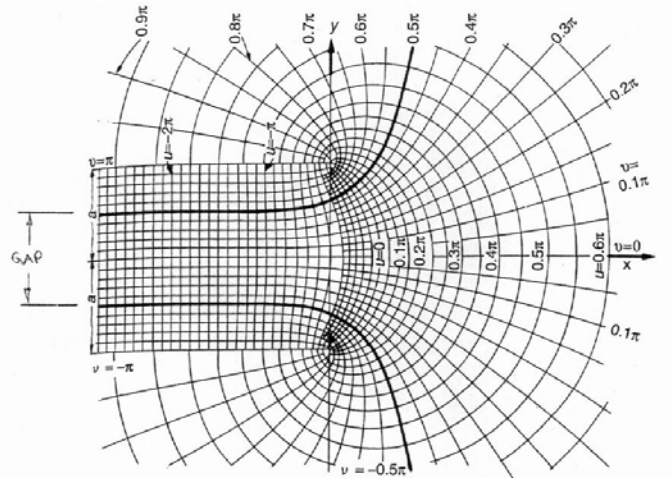
HV Electronics Boards

- Avoid HV on PCB traces
  - Air gaps in adjacent laminations
  - Small traces with sharp edges => high fields
- HV leads:
  - Elevate large diameter wires above board on suitable standoffs
  - Use large, uniform solder balls – no points
- Graduate HV from one end of board to other
- Thin-walled dielectric shell around HV circuits (optional)
  - Plated as Faraday cage on outer surface (or similar arrangement)
- Vacuum encapsulation (optional)
- Field control loops around HV zones (optional)



Misc Comments, p1

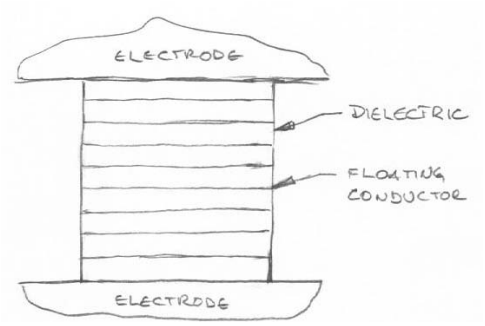
- Magnetic fields can direct charge flow to advantage
  - Has other issues, use great care
- Perfect edge termination for parallel electrodes:
  - Rogowski contour. Not practical in most cases
  - Suitable radius provides pretty close approximation
    - Edge radius = gap => max field only ~10% higher than E_0
    - Also usually not practical: too large & massive



Rogowski contours (heavy lines)
from Kuffel, Zaengl & Kuffel

Misc Comments, p2

- A perfect termination for coax cables?
  - Pretty good (“stress cone”), but not unique
  - Various trade-offs
- Avoid floating conductors that can charge up and discharge like capacitors
  - Some exceptions
    - Capacitors with floating layers control fields well



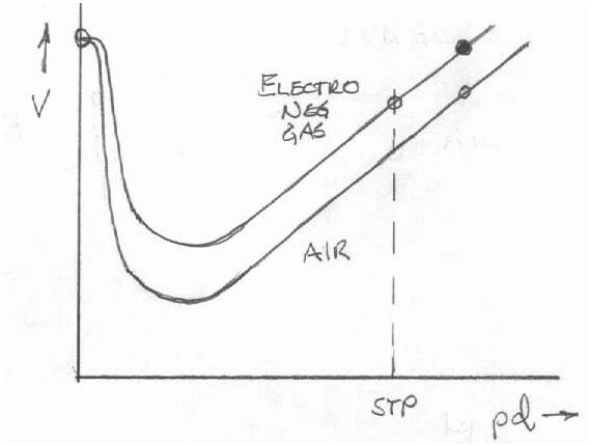
Multi-Layer ceramic capacitor stack
with floating conductive layers

HV at Atmospheric Pressure, p1

- All space HV test systems include elements
  - In vacuum, and
  - In air
- Design for both
  - Particularly at interfaces: connectors and vacuum feed-throughs
- In air
  - Minimize dust
  - Eliminate air drafts
  - Use HV rods and balls, if called for

HV in Ambient Atmosphere, p2

- Elelctro-negative gasses (electron collectors)
  - At STP, less prone to discharge than air
  - Characterized by “Breakdown Voltage Multiplier” (BVM)
    - Freon = 2.4
    - Sulphur hexafluoride = 2.3
    - Carbon Tetra-chloride = 6.3
  - Elevated pressure also helps
    - 5 atmospheres of SFl_6 = 12
- Possible applications
  - Vacuum sealed HVPS container
    - Filled with pressurized electro-negative gas
    - Issues: leakage to Paschen minimum, electrical interfaces through walls
    - Loss of vacuum due to outgassing leaks
  - Just evacuated container – many issues



Dangers, p1

- HV is **DANGEROUS – things go wrong!**
- Life is threatened by current, not voltage:
  - Much more at shown site
- Know your power supply's characteristics
  - If it SHUTS OFF with over-current
    - Equivalent to a circuit breaker
    - This is SAFE
  - If it is power limited
    - V will sag as i continues to rise?
    - Dangerous!

Electric Current (1 second contact)	Physiological Effect
1 mA	Threshold of feeling, tingling sensation.
5 mA	Accepted as maximum harmless current
10-20 mA	Beginning of sustained muscular contraction ("Can't let go" current.)
100-300 mA	Ventricular fibrillation, fatal if continued. Respiratory function continues.

From: http//:hyperphysics.phy-astr.gsu.edu/hbase/electric/shock.html

- Use a protection resistor in line located immediately at the PS output, if possible
  - Old carbon resistors are better than new metal film resistors
  - Best encapsulated

Dangers, p2

- Follow the standard rules:
  - Keep one hand in pocket
  - Remove conductive jewelry (rings, watches)
  - Stand away from equipment racks and other conductors
  - Wear dry, rubber soled shoes
  - Don’t stand in water
    - For example, in puddles from LN2 delivery systems by vacuum chambers
  - Have a second person present

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More: Eric Hertzberg on High Voltage Field Analysis Techniques and Associated Software

Introduction to Electro-Magnetic Field Solvers

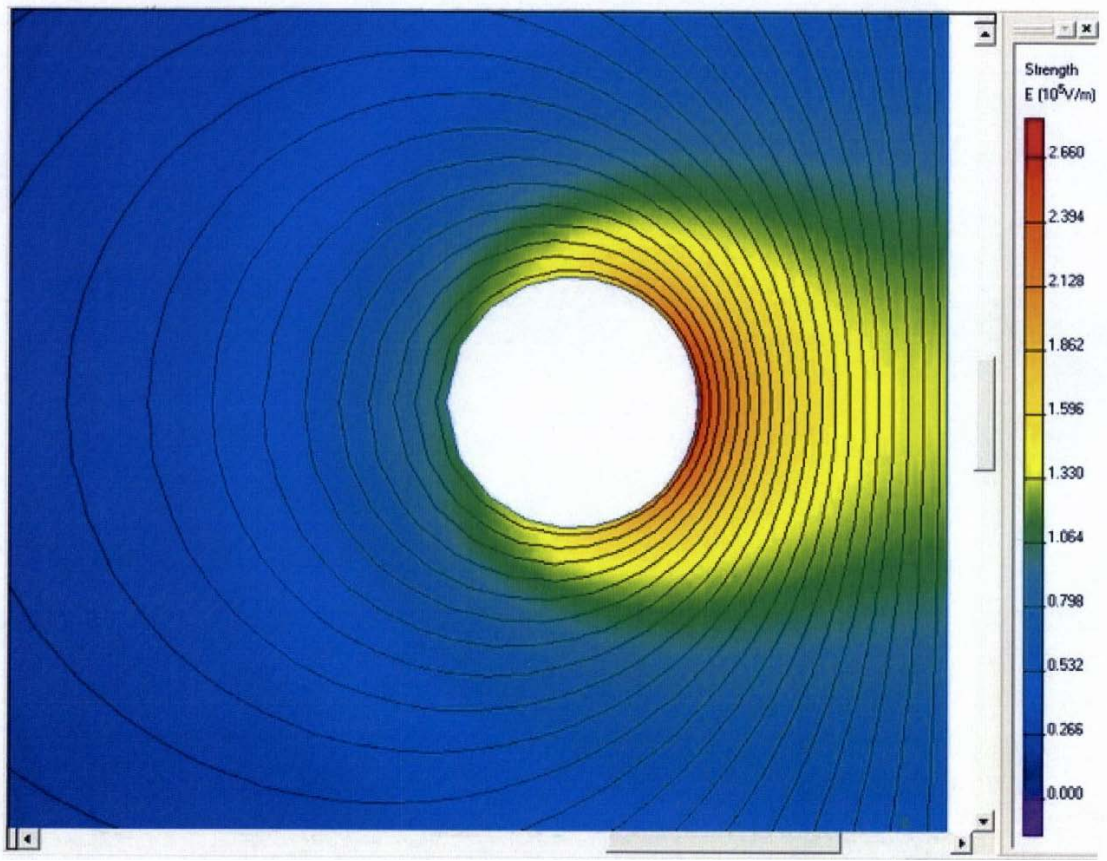
Eric Hertzberg and Tom Sanders

Lockheed Martin Advanced Technology Center, Palo Alto, CA

General Comments

- Electro-Magnetic Field solvers
  - Powerful computerized analytical tools that calculate electro-matnetic field properties based on
    - Boundary conditions
    - Materials properties
  - Nearly all solution methods derive from finite element mathematics & technology
  - All are a subset of the broader category of
    - Boundary Value Problem solvers for physics
- Substantial software selection decision tree

Field Plot



Field solution for a conductive sphere near a conductive plane with voltage between.
From website: [http://www.nessengr.com/techdata/fields/field.html]

Boundary Considerations, p1

- Boundary Inputs
  - Scale size and physical shape
    - Sub-atomic to intergalactic
      - Atomic/molecular scales (quantum mechanical)
      - Integrated Circuit feature and component scales (10 of nm's)
      - Practical S/C instrument field sizes (1 mm - 30 cm)
      - Antennas (cm's to 10s of m's)
      - Signal transmissions (100's of km to vastly larger (radio telescopy))
  - Time domain phenomena
    - Static (DC)
    - Changing, Periodic - All EM wavelengths
    - Changing, Non-Periodic - Pulsed, spiked, random, etc

Boundary Considerations, p2

- Materials properties
  - Widely variable properties
    - Temperature
    - Spin, Velocity
    - Time degradation
    - Adsorbed gas layers, etc.
  - “Constants”
    - Dielectric constant
    - Resistivity
    - Magnetic permeability
    - Index of refraction
    - Thermal expansion, stability, etc.

Engineering Issues

- Desired Outputs
  - Scalar values, 2D & 3D representations
  - Vector fields, 2D & 3D representations and matrices

Program Decisions, p1

- Developers went in many directions
  - Generalized programs:
    - Moderate capability: Field solving only, 2D RS or 3D
      - 2D RS = 2D plus Rotational Symmetry only, but NOT full 3D
      - Often called 2-1/2 D
    - High capability: 3D Field Solving
    - Higher capability: Field Solving plus ray tracing
    - Highest capability: “Multi-physics software”
      - Extremely powerful - go far beyond merely solving EM fields
      - Prepare outputs for follow-on analyses
        - » Space charge limitation studies
        - » Shock phenomena, etc

Program Decisions, p2

- Diverse specialized programs
  - Explicitly tailored and optimized to the particular problem at hand
    - Seeking ever higher speeds for increasingly complex problems
    - Commercial packages focused on certain design areas (motors, etc)
  - Combinations of above with various add-on packages

Practical Considerations, p1

- Cost
- ITAR restrictions on support for foreign products
- Learning curve; ease of use
  - Input/ Output Formatting
- Ease of customization/ adaptation of software
- Required computational hardware/web resources
  - Computer speed and memory
- Math process efficiency (speed)
- Model precision at boundaries (seldom exact)

Practical Considerations, p2

- Meshing management
  - Regular meshing
    - Cubic, tetrahedral or similar everywhere
  - Conformal meshing
    - Locally shaped to match physical boundary features
  - Adaptive meshing
    - Mesh size is automatically adjusted locally to match
      - Physical features
      - High field intensity zones
    - Meshes are finer only where needed
      - Lower memory - higher speed - greater accuracy

Practical Considerations, p3

- Entry of geometry
  - Custom hand entry
  - Commercial 3D model entry
    - Compatibility with supporting software
      - 2D or 3D CAD packages
      - AutoCad, Pro-E, SolidWorks, Katia, etc
    - Combination of custom and commercial
  - Entry of geometry-dependent field input data (thermal fields, etc)
  - Post-processing of outputs - compatibility with
    - MathCad, Mathematica, etc

- ONE SIZE DOES NOT FIT ALL!
  - User must know WANTS, tempered by NEEDS

Field Solver Software, p1

- Focused on needs for miniaturized space instruments
  - Unit size: roughly 1 to 30 cc
  - HV gap width and feature size: typically 1 to 20 mm
  - Voltages
    - Usually <10 kV, DC and/or stepped
      - Total step transition speeds: between m seconds and 1 second
    - Sometimes up to 25 kV DC
    - No RF
      - Any inclusion here is incidental and limited

Field Solver Software, p2

- Low cost, relatively easy to learn
  - QuickField (headquartered in Denmark)
    - 2D RS E or M and time variable solvers
  - Maplesoft (headquartered in Canada)
    - 2D RS E or M solvers
  - SIMION (Software Information Systems (SIS), Louisville, KY)
    - 2D RS EM and 3D E field solvers
  - SIMION combined with other extension packages
    - Such as Aston Labs, Purdue Univ.
    - 2D RS EM field solvers with ray tracing

Field Solver Software, p3

- Higher cost, more intricate to learn
  - Integrated Engineering Software (EIS) (headquartered in Canada)
    - Many levels of E or M, EM and time domain field solvers
      (ELECTRO, COULOMB, SINGULA, CHRONOS, MAGNETO, AMPERES, OERSTED, FARADAY, INDUCTO)
    - LORENTZ – premier E or M, EM and time domain field solvers
      - all with ray tracing
  - CST (Computer Simulation Technology), (headquartered in Germany)
    - EM Studio - static and low frequency EM field solver
    - EM Particle Studio (plus other modules) - 3D EM field solver and ray tracer
  - ANSYS
    - Maxwell - 2D & 3D EM field solver
    - Multi-physics - field solver, ray tracer and much more
  - COMSOL
    - Multi-physics - 3D EM field solver and much more
    - Multi-physics plus Particle Tracing, other modules- 3D EM field solver, ray tracing

Field Solver Services

- Dr. Arthur Ghielmetti, US citizen and resident of Switzerland,
  - Personally written field solver
    - Can incorporate SIMION
  - 2D RS EM field solving with full 3D ray tracing and some RF capability
  - Automated optimization
  - Proven high accuracy at boundaries
  - Decades long record of successes in space instrumentation

Closing Comments

- MANY MORE
  - When RF is part of the design, there is an additional long list of tailored programs
    - Search on Google
  - Many universities have in-house-developed field solvers and multi-physics packages
    - Highly specialized and optimized
    - Focused capabilities and limitations;
    - Some have incorporated iterative design-optimization capabilities
    - Compatibilities with commercial packages

Cautions

- BEWARE:
  - Very easy to get tripped up
    - Achieve plausible but incorrect answers
  - For confidence, one must have guidance from someone knowledgeable with the
    - Applicable physics
    - Software architecture, capabilities and limitations